SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 3/15/2004 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 272-2511.

Date 5/3/04 Serial # 09/891,787 Priority Application Date _____

Your Name M. Lewis Examiner # _____

AU 2829 Phone 272-1838 Room 5A30

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

05-03-04 P02:44

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____

Secondary Refs ✓ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-28

Problem: See Paragraphs 1 & 2

Solution: " " 3-5

Staff Use Only

Searcher: Speckhard

Searcher Phone: _____

Searcher Location: STIC-EIC2800, JEF-4B68

Date Searcher Picked Up: 5/5/04

Date Completed: 6/5/04

Searcher Prep/Rev Time: 180

Online Time: 160

Type of Search

Structure (#)_____

Bibliographic ✓

Litigation_____

Fulltext_____

Patent Family ✓

Other all.

Vendors

STN_____

Dialog ✓

Questel/Orbit_____

Lexis-Nexis_____

WWW/Internet_____

Other _____

STIC Search Report
EIC 2800

STIC Database Tracking Number: 120988

TO:	From:
Monica Lewis **Location: JEF 5A30** **Art Unit : 2822** **Thursday, May 06, 2004** **Case Serial Number: 09/891727**	**Irina Speckhard** **Location: EIC 2800 JEF 4B59** **Phone: (571) 272-2554** **irina.speckhard@uspto.gov**

Search Notes

Examiner Lewis,

Please find attached first-pass prior-art search results from the patent and non-patent abstract databases. The results were based on claims and statements of technical problems and solutions. Tagged records might be worth your review as well as the rest of the references provided.

If you need further searching or have questions or comments, please let me know.

Thank you,

Irina Speckhard

STIC Search Results Feedback Form

EIC 2800

Questions about the scope or the results of the search? Contact ***the EIC searcher or contact***:

Jeff Harrison, EIC 2800 Team Leader
571-272-2511, JEF 4B68

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2810*
- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

  Types of relevant prior art found:
  - ☐ Foreign Patent(s)
  - ☐ Non-Patent Literature
    (journal articles, conference proceedings, new product announcements etc.)
- *Relevant prior art **not found**:*
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2800, CP4-9C18

05may04 15:43:00 User267149 Session D1376.1

SYSTEM:OS - DIALOG OneSearch
File 2:INSPEC 1969-2004/Apr W4
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File 315:ChemEng & Biotec Abs 1970-2004/Apr
(c) 2004 DECHEMA
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200427
(c) 2004 Thomson Derwent
*File 350: For more current information, include File 331 in your search. Enter HELP NEWS 331 for details.
File 347:JAPIO Nov 1976-2003/Dec(Updated 040402)
(c) 2004 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.
File 344:Chinese Patents Abs Aug 1985-2004/Mar
(c) 2004 European Patent Office
File 371:French Patents 1961-2002/BOPI 200209
(c) 2002 INPI. All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.

Set	Items	Description
S1	4256	LATERAL?(3N)CONDUCT?
S2	8472	CONDUCT?(3N)(SUPERJUNCT? OR SUPER()JUNCT? OR JUNCT?)
S3	12707	S1:S2
S4	2618974	SEMICONDUCT?
S5	2756	MOSGATE???? OR MOS()GATE???
S6	96815	GATE???(3N)((MICRO)()(ELECTRONIC? OR CIRCUIT? ? OR CHIP? ?) OR CHIP? ? OR MICROCIRCUIT? ? OR DIE? ? OR LOGIC()CIRCUIT? ? OR WAFER? ? OR MICROELECTRONIC OR DICE OR ELECTRODE? ?)
S7	99170	S5:S6
S8	4832244	TRENCH? OR HOLE? OR GROOVE? OR CHANNEL OR EDGE? OR FLUSH OR RIDGE?
S9	75072	(TRENCH? OR HOLE? OR GROOVE? OR CHANNEL OR EDGE? OR FLUSH - OR RIDGE?)(3N)(VERTICAL? OR UPRIGHT OR SPACED OR SPACE OF SPACING)
S10	2209	(TRENCH? OR HOLE? OR GROOVE? OR CHANNEL OR EDGE? OR FLUSH - OR RIDGE?)(3N)(MESA OR MESAS)
S11	109516	(DEPTH OR DEEP??? OR CONCENTRAT? OR THICK?)(3N)(TRENCH? OR HOLE? OR GROOVE? OR CHANNEL OR EDGE? OR FLUSH OR RIDGE? OR MESA OR MESAS)
S12	4832686	S8:S11
S13	4691784	DIFFUS? OR SCATTER? OR DISSEMINAT? OR DISPERS? OR SPREAD?
S14	856	RESURF OR REDUC?()SURFACE()FIELD
S15	80481	(DRAIN OR SOURCE)(3N)(REGION? ? OR AREA? ?)
S16	342326	(UPPER OR TOP)(3N)SURFAC?
S17	35017	(VOLT? OR POTENTIAL)(3N)CONDITION?
S18	2876	S3 AND S4
S19	156	S18 AND S7
S20	88	S19 AND S12
S21	21	S20 AND S13
S22	1	S21 AND S14
S23	20	S21 NOT S22
S24	10	S23 AND S15
S25	10	RD (unique items)
S26	10	S23 NOT S24
S27	0	S26 AND S16
S28	10	RD S26 (unique items)
S29	67	S20 NOT S21
S30	4	S29 AND S5
S31	4	RD (unique items)
S32	63	S29 NOT S30
S33	4	S32 AND S9
S34	4	RD (unique items)
S35	59	S32 NOT S33
S36	0	S35 AND S17
S37	0	S35 AND S10
S38	2	S35 AND S11
S39	2	RD (unique items)
S40	57	S35 NOT S38
S41	24	S40 AND S1
S42	0	S41 AND S2
S43	0	S41 AND S13
S44	0	S41 AND S5
S45	24	S41 AND S6
S46	22	RD (unique items)
S47	22	S46 AND S8

S48	22	S47 AND S4
S49	35864	S7 AND S12
S50	24	S49 AND S14
S51	21	S50 NOT S21,S30,S33,S38,S45
S52	0	S51 AND S3
S53	17	S51 AND S4
S54	8	S53 AND S13
S55	7	RD (unique items)
S56	9	S53 NOT S54
S57	0	S56 AND S10
S58	0	S56 AND S11
S59	8	RD S56 (unique items)
S60	47	S14 AND S7
S61	23	S60 NOT S21,S30,S33,S38,S45,S50
S62	0	S61 AND S12
S63	18	S61 AND S4
S64	0	S63 AND S3
S65	1	S63 AND S17

22/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015160132
WPI Acc No: 2003-220660/200321
XRPX Acc No: N03-176074

Lateral superjunction **semiconductor** device for use as high side switch, has **trenches** with **mesas** and N **diffusion** lines with **reduced surface field** concentration of prescribed width and concentration

Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: KINZER D M; SRIDEVAN S

Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020195627	A1	20021226	US 2001891727	A	20010626	200321	B
DE 10229146	A1	20030109	DE 1029146	A	20020628	200321	
JP 2003115588	A	20030418	JP 2002186923	A	20020626	200335	

Priority Applications (No Type Date): US 2001891727 A 20010626
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020195627	A1		10	H01L-031/62	
DE 10229146	A1			H01L-029/78	
JP 2003115588	A		22	H01L-029/78	

Abstract (Basic): US 20020195627 A1
Abstract (Basic):

NOVELTY - **Trenches** (20-23) extending through P-region (13) into top of N region (12), has mesas of prescribed width and concentration. N **diffusion** lines (30) having **reduced surface field** (**RESURF**) concentration, is **diffused** into the walls and along the bottom of **trenches**. A **gate electrode**, source and base regions of a **MOS gate** structure is connected at one end of the **trenches** and drain of the **MOS gate** structure is connected to other end.

USE - Lateral superjunction **semiconductor** device e.g. MOSFET for use as high side switch.

ADVANTAGE - Since the **trenches** with **mesas** and N **diffusion** lines with **RESURF** concentration have prescribed thickness and concentration, during the application of voltage to drain, the mesas and N **diffusion** fully deplete under blocking voltage conditions, and thus allows an almost uniform electric field distribution along the **trench** length. By the use of **resurf** concentration, the voltage applied between the drain and source on the device withstands.

DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view of the **lateral conductive superjunction semiconductor** device.

n region (12)
p region (13)
Trenches (20-23)
N-**diffusion** lines (30)
pp; 10 DwgNo 3/12

Trenches (3)
Diffusion (4)
pp; 15 DwgNo 2/3

25/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013406398
WPI Acc No: 2000-578336/200054
Related WPI Acc No: 1998-505681
XRPX Acc No: N00-427886
MOSFET for large scale integration circuits, has **gate electrode** with highly doped, highly conductive inner region and lower conductance **edge** which overlap between electrode and active region
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: DUANE M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6091118	A	20000718	US 97780615	A	19970108	200054 B
			US 98103699	A	19980624	

Priority Applications (No Type Date): US 97780615 A 19970108; US 98103699 A 19980624
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6091118	A		8	H01L-029/76	Div ex application US 97780615 Div ex patent US 5804496

Abstract (Basic): US 6091118 A
Abstract (Basic):
NOVELTY - **Gate electrode** (205), disposed on the substrate (201), has a highly doped and highly conductive inner region and lower conductance **edge** portion which overlap an adjacent active region. The dopant inhibits **diffusion** of the gate dopant which has different conductivity type than gate dopant.
USE - For large scale integration circuits.
ADVANTAGE - Reduces the overlap capacitance and increase the performance of **semiconductor** without significantly impacting the field effect in the **channel** region. By implanting through a spacer, higher penetration of the active region with **edge** dopant is achieved, thereby reducing the lateral **diffusion** of the source/drain implants. Reduced **conductance edge** portions have **lateral** width comparable in length to **gate electrode**-source/drain overlap which improves transistor performance by reducing the capacitance between the **gate electrode** and **source/drain region** without degrading the drive current of the transistor.
DESCRIPTION OF DRAWING(S) - The figure illustrates the fabrication process of a **semiconductor** device having reduced overlap capacitance.
Substrate (201)
Gate electrode (205)
pp; 8 DwgNo 2F/5

25/3,AB/3 (Item 3 from file: 350)

008645905
WPI Acc No: 1991-149934/199121
XRAM Acc No: C91-064817
XRPX Acc No: N91-115132

Reduced effect of contact-window mis-alignment in integrated circuits - using spacer technique inside the contact window to restrict interaction of interconnect layer with **diffusion** to a smaller area

Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)
Inventor: MOTONAMI K; SUIZU K

Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4035991	A	19910516	DE 4035991	A	19901112	199121	B
JP 3218626	A	19910926	JP 90268230	A	19901004	199145	
US 5309023	A	19940503	US 90609561	A	19901106	199417	
			US 92888323	A	19920526		
DE 4035991	C2	19940623	DE 4035991	A	19901112	199423	
KR 9309016	B1	19930918	KR 9017341	A	19901029	199436	

Priority Applications (No Type Date): JP 90268230 A 19901004; JP 89296832 A 19891114
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5309023	A		14	H01L-023/48	Cont of application US 90609561
DE 4035991	C2		21	H01L-021/283	
KR 9309016	B1			H01L-023/52	

Abstract (Basic): DE 4035991 A

In a contact window (103), formed by etching through an insulator layer (2) to allow contact between the metallisation-layer (191) and a **diffused** region (113), pref. containing a lightly doped **drain** (LDD) **region**, resistant spacers (151) are present. The spacers restrict the area of interaction between the metallisation layer and the **diffusion** to the central region of the contact. The spacers are pref. made of a conductive or an insulating material, pref. undoped polycrystalline Si. The metallisation layer pref. consists at least partly of a doped poly-Si layer, while the spacers present a higher resistance to **diffusion** of these impurities than the substrate does in vertical direction.

Also claimed is a metallisation layer contg. a refractory metal. In this case the spacers prevent interaction between the metal and the substrate except in the central area of the contact.

The spacers are pref. mfd. by deposition of a poly-Si layer over the device surface after the contact window formation and controlled anisotropic etch-back. The metallisation layer is then completed by deposition of an undoped poly-Si layer followed by doping, of a doped poly-Si layer or of a refractory metal layer.

USE/ADVANTAGE -The spacers reduce the lateral **diffusion** or siliciding in the contact window, which allows the contact window to be placed closer to the LDD region or allows increased alignment tolerance. The contact window pref. has a ratio of dia. to layer-thickness of not more than 1. The spacer width from window **edge** to **edge** of the spacer is 150-200 nm. The process is used in the mfr. of Si integrated circuits, pref. DRAMs.

Dwg.7/13

Abstract (Equivalent): US 5309023 A

A contact structure for interconnection in FET devices comprises: a **semiconductor** substrate having a main surface; a conductive region formed in the **semiconductor** substrate; an insulating layer formed on the main surface of the **semiconductor** substrate and having a contact **hole** formed to reach a surface of the conductive region; a **gate electrode** formed within the insulating layer; an interconnection layer formed on the surface of the conductive region and over the insulating layer and comprising a high melting point material as a main material; and means for restraining an impurity **diffusion** region caused by interaction between the interconnection layer and the **conductive** region from extending **laterally** from the contact **hole** into the **semiconductor** substrate. The means for restraining has a higher resistivity to interaction with the conductive region than the interconnection layer, and is formed as a distinct structure from the interconnection layer and arranged on the conductive region between the interconnection layer and the conductive region entirely within the contact **hole** as defined by the insulating layer.

ADVANTAGE - Characteristics of the conductive region are not deteriorated even when errors have occurred in the patterning for forming contact **hole**.

Dwg.2/10

25/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008490842
WPI Acc No: 1990-377842/199051
XRAM Acc No: C90-164589
XRPX Acc No: N90-287963

Mfg. silicon field effect power **semiconductor** device - includes forming low sheet resistance tungsten silicide-polysilicon-oxide **gate electrode** stack

Patent Assignee: GENERAL ELECTRIC CO (GENE)
Inventor: BALIGA B J; KORMAN C S; PIACENTE P A; SHENAI K

Number of Countries: 007 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 403113	A	19901219	EP 90305911	A	19900531	199051	B
US 4985740	A	19910115	US 89359811	A	19890601	199106	
JP 3068657	A	19910325	JP 90141749	A	19900601	199118	
JP 3082043	A	19910408	JP 90141751	A	19900601	199120	

Priority Applications (No Type Date): US 89359811 A 19890601
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 403113	A				

Designated States (Regional): DE FR GB IT SE

Abstract (Basic): EP 403113 A

Device is mfd. by : oxidising the surface of a wafer doped first type; depositing polySi on the resulting oxide; adding a WSi layer; antisotropically etching the resulting silicide/polySi/oxide stack to define a WSi **gate electrode** layer with an aperture in it; and forming in the wafer through the aperture an active device by implanting and **diffusing channel** and **source regions**.

The wafer is pref. capped with thin thermal oxide after

implantation but before **diffusion**; **diffusion** is performed at above 1000 deg.C. The WSi layer is an LPCVD layer. The etching is a two-stage reactive ion etching step, pref. using CBrF3 to remove WSi and Cl2 to remove the remainder, or alternatively, using SF6 and HCl respectively. The implanted ion is As.

ADVANTAGE - The WSi/poly/oxide gate layer stack has low sheet resistance and good frequency response. (claimed). (21pp Dwg.No.2/3

Abstract (Equivalent): US 4985740 A

A new multi-cellular power field effect **semiconductor** device comprises a body (110) of Si **semiconductor** material with N+ **drain region** (114) adjacent the lower surface (112) and N-drift **region** (116) above the **drain region**. Body **region** (118) of P-type material extends into the drift region from the upper surface (111) of the body and N+ **source region** (120) extends into the body region from the upper surface (111), on which an insulated gate structure (131) is formed.

Gate electrode comprises an insulating layer (130) on the surface and a conductive polycrystalline Si layer (132) on the oxide. W silicide layer (134) is formed on the poly-Si layer to provide high **lateral conductivity**. W layer (136) contacts the **source region** (120) where it extends to the surface within the aperture defined by the **gate electrode**. ADVANTAGE - Improved on-resistance and lowered ohmic contact resistance are obtd. (18pp

25/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004391280
WPI Acc No: 1985-218158/198536
XRAM Acc No: C85-095015
XRPX Acc No: N85-163893
MOSFET suppressing parasitic bipolar transistor - by source, trunk and drain zones in series, an auxiliary and one **channel** zone
Patent Assignee: GENERAL ELECTRIC CO (GENE); RCA CORP (RADC)
Inventor: GOODMANN A M; GOODMANN L A; GOODMAN A M; GOODMAN L A
Number of Countries: 008 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3505393	A	19850829	DE 3505393	A	19850216	198536	B
GB 2154794	A	19850911	GB 854367	A	19850220	198537	
FR 2559958	A	19850823	FR 852448	A	19850220	198540	
JP 60202967	A	19851014	JP 8534285	A	19850221	198547	
US 4587713	A	19860513	US 84582601	A	19840222	198622	
GB 2154794	B	19871231				198801	
US 4837606	A	19890606	US 8714196	A	19870212	198928	
DE 3505393	C2	19950622	DE 3505393	A	19850216	199529	

Priority Applications (No Type Date): US 84582601 A 19840222; US 85798612 A 19851115
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3505393	A		22		
DE 3505393	C2		8	H01L-029/772	

Abstract (Basic): DE 3505393 A

A vertical double-**diffused** MOSFET with source, trunk and drain zones of alternating n-type and p-type, sepd. by pn-junctions,

has on the first principal surface a source electrode and on the opposite principal surface a drain electrode. An auxiliary zone of the p-type trunk zone passes sideways under at least a part of the **channel** zone and has a higher dopant concn. than the trunk zone.

ADVANTAGE - This reduces the effects of the parasitic bipolar transistor within a VDMOS module and lowers the ON or contact resistance. Its threshold voltage is lower than with similar known modules.

2/3

Abstract (Equivalent): DE 3505393 C

Prodn. of FET comprises: (a) providing **semiconductor** body (52); (b) forming mask on main surface (54); (c) forming base zone (62) and drain-pn junction (64); and (d) **diffusing** dopant of 1st conducting type (N) through mask to form source zone (66). By implanting dopant of 2nd conducting type (P), an auxiliary zone (80) is produced extending below a part of the **channel** zone (70).

ADVANTAGE - Improved resistance.

Dwg.1/3

Abstract (Equivalent): GB 2154794 B

A vertical MOSFET device comprising a **semiconductor** wafer including, in series, **source**, body and **drain regions** of alternate **conductivity** type having PN **junctions** therebetween, the **source** and **drain regions** being spaced so as to laterally define a **channel** region in the body region at a first surface of the wafer a source electrode on said first surface of said wafer and drain electrode on an opposing surface of said wafer, and a supplementary region of similar conductivity type to said body region, said supplementary region having a high areal dopant concentration compared to that of said body region and extending laterally beneath at least a portion of said **channel** region.

Abstract (Equivalent): US 4837606 A

Vertical MOSFET device comprises a) a **semiconductor** wafer having first and second opposing major surfaces; b) a first conductivity type **drain region** at the first surface; c) a second conductivity type **drain region** extending from the first surface so as to form a PN junction with the **drain region**; d) a first conductivity type **source region** extending a predetermined depth into the body region so as to form a source/body PN junction, the spacing between the source/body PN junction and the body/drain PN junction defining a **channel** region in the body region at the first surface; e) a source electrode contacting the **source** and body **regions** at the first surface; f) an insulated **gate electrode**; and g) a drain electrode on the second surface.

The improvement is that the device has h) a second conductivity type supplementary region contiguous with the body region and having a high areal dopant concn compared to that of the body region. Region h) includes a region of peak dopant concn that is parallel to the first surface at a predetermined depth from it, and extends laterally beneath at least part of the **channel** region.

ADVANTAGE - The effects of the parasitic lipolar transistor are even more effectively reduced. (7pp)

US 4587713 A

Prodn. of a VDMOS device is effected using a **semiconductor** wafer with a **drain region** adjacent to the surface. A second conductivity type dopant is **diffused** into the wafer using a mask aperture. This forms a body **region** and a body/**drain** PN junction.

A further dopant of the first type is **diffused** via the aperture to form a **source region** and a **source**/body PN

junction.

Process is improved by implanting a supplementary second type dopant via the aperture and annealing to create a further region of high dopant concentration, extending under part of the **channel** region.

ADVANTAGE - Device operates with a low threshold voltage and the parasitic effects of a bipolar transistor are reduced. (7pp)D

25/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004099232
WPI Acc No: 1984-244773/198440
XRAM Acc No: C84-103316
XRPX Acc No: N84-183102
MOSFET-diode device - with multiple pad-to-base connections to avoid drop-outs
Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: LIDOW A
Number of Countries: 011 Number of Patents: 011
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3410427	A	19840927	DE 3410427	A	19840321	198440	B
GB 2137811	A	19841010	GB 846974	A	19840316	198441	
FR 2543366	A	19840928	FR 844410	A	19840321	198444	
SE 8401090	A	19840922				198445	
JP 59214254	A	19841204	JP 8454137	A	19840321	198503	
GB 2137811	B	19870107				198701	
US 4789882	A	19881206	US 83477012	A	19830321	198851	
DE 3410427	C	19900201				199005	
IT 1173885	B	19870624				199023	
KR 8904548	B	19891113				199043	
JP 6318708	A	19941115	JP 8454137	A	19840321	199505	
			JP 93163306	A	19840321		

Priority Applications (No Type Date): US 83477012 A 19830321
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3410427	A		19		
JP 6318708	A		11	H01L-029/784	Div ex application JP 8454137

Abstract (Basic): GB 2137811 A

A metal oxide **semiconductor** field effect transistor comprising a **semiconductor** wafer, a plurality of base regions of one **conductivity** type symmetrically and **laterally** distributed over at least a portion of the area of one surface of said wafer; a respective **source region** of the other conductivity type formed in each of said base regions at a position laterally spaced from the periphery of said respective base regions which **channel** regions are capable of inversion; an insulation layer overlying each of said **channel** regions and extending over a connection pad region; and conductive gate means disposed atop said insulation layer over each of said **channel regions**; a **source** electrode means in contact with each of said **source regions** and with each of said base **regions**; a **drain** electrode connected to the opposite surface of said wafer; an enlarged **area source** electrode pad connected to said source electrode means and overlying said insulation layer in said connection pad region; an enlarged area

base region of said one conductivity type underlying said source electrode pad; and connection means electrically connecting at least portions of the periphery of said source electrode pad to said enlarged base region beneath said pad whereby said enlarged base region can efficiently collect minority carriers when said transistor operates as a diode.

DE 3410427 A

A high power MOSFET includes connections (80,81,82) which connect at least part of the periphery of the source-electrode-contact pad with the enlarged base region (20) below the pad so that the enlarged base region can collect minority carriers when the MOSFET operates as a diode.

Also claimed is a **semiconductor** component with a number of separate parallel-connected diode elements, formed in a common substrate of first conductivity type, and an enlarged electrode contact pad connected with each diode element. Each diode element includes a **diffusion** region of opposite conductivity type which forms a boundary layer in the substrate. A further **diffusion** region of opposite conductivity type lies below the electrode pad. A thin insulation layer separates the insulation layer and the substrate in the region of the electrode pad. Several electrical connection regions extend from the electrode pad to the second enlarged base region and are formed around at least part of the periphery of the source-**electrode** which surrounds the **gate-electrode**-contact pad device.

ADVANTAGES - No drop-outs or component breakdowns occur on diode operation.

Dwg.2/4

Abstract (Equivalent): GB 2137811 B

A metal oxide **semiconductor** field effect transistor comprising a **semiconductor** wafer, a plurality of base regions of one **conductivity** type symmetrically and **laterally** distributed over at least a portion of the area of one surface of said wafer; a respective **source region** of the other conductivity type formed in each of said base regions at a position laterally spaced from the periphery of said respective base regions which **channel** regions are capable of inversion; an insulation layer overlying each of said **channel** regions and extending over a connection pad region; and conductive gate means disposed atop said insulation layer over each of said **channel regions**; a **source** electrode means in contact with each of said **source regions** and with each of said base **regions**; a **drain** electrode connected to the opposite surface of said wafer; an enlarged **area source** electrode pad connected to said source electrode means and overlying said insulation layer in said connection pad region; an enlarged area base region of said one conductivity type underlying said source electrode pad; and connection means electrically connecting at least portions of the periphery of said source electrode pad to said enlarged base region beneath said pad whereby said enlarged base region can efficiently collect minority carriers when said transistor operates as a diode.

Abstract (Equivalent): US 4789882 A

Metal oxide **semiconductor** field effect transistor (I) comprises (A) a **semiconductor** wafer; (B) a plurality of base regions of one **conductivity** type symmetrically and **laterally** distributed over a least a portion of the area of one surface of (A), the portion of (A) receiving base regions (B) being of the other conductivity type; (C) a respective **source region** of the other conductivity type in each of regions (B) being laterally spaced from the periphery of their respective base regions (B), to

define respective annular **channel** regions capable of inversion within their respective base region (B); (D) an enlarged area base region of the said one **conductivity** type being **laterally** displaced from regions (B) and extending to the said one surface of (A); (E) an insulation layer overlying each of the **channel** regions and extending over region (D); (F) conductive **gate electrode** means disposed atop layer (E) and over each of the **channel regions**; (G) a **source** electode means in contact with each of the **source regions** (C) and in contact with each of base **regions** (B); (H) a **drain** electrode connected to the opposite surface of (A); (I) an enlarged area souce electode pad, continuous with means (G) and overlying the insulation layer which extends over region (D), pad (I) having a peripheral region disposed adjacent means (G); and (J) a plurality of spaced connection means connecting respective portions of pad (I) adjacent to the periphery to region (D) beneath the pad. The peipher to region (D) beneath the pad. The enlarged base region (D) can efficiently collect minority carriers when the base regions are forward biased relative to the portion of (I) which receives the pluality of base regions (B).

ADVNTAGE - NoVel connection is provided of the peripheries of the electrode pads of transistors (I), directly to the underlying silicon, to prevent failure of the device when operated in a diode mode.

(6pp

25/3,AB/7 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05890084
LATERAL CONDUCTION MODULATING MODE MOSFET

PUB. NO.: 10-173184 [JP 10173184 A]
PUBLISHED: June 26, 1998 (19980626)
INVENTOR(s): NAKAGAWA AKIO
YAMAGUCHI YOSHIHIRO
WATANABE KIMINORI
OHASHI HIROMICHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 09-242729 [JP 97242729]
FILED: September 08, 1997 (19970908)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce the resistance of the base layer present below the **channel** region of a MOSFET and prevent its latchup, by so disposing an exposed portion of its high-resistance layer to its wafer surface as to have island-form patterns enclosed completely by the base layer.

SOLUTION: Forming an n(sup -)-type high-resistance layer 32 on a P(sup +)-type layer 31, a P-type base **diffusion** layer 33 is formed selectively in the surface portion of the n(sup -)-type high-resistance layer 32. Hereupon, the **diffusion** patterns of the P-type base **diffusion** layer 33 and the n(sup -)-type high-resistance layer 32 are so formed that an exposed portion of the n(sup -)-type high-resistance layer 32 to the wafer surface of a MOSFET has island-form patterns enclosed completely by the P-type base fiffusion layer 33. Then, n(sup +)-type source **diffusion** layers 34 are formed selectively in the surface portion of the base **diffusion** layer 33, and a **gate electrode** 36 is disposed via a gate insulation layer 35 on the P-type

diffusion layer portion 33 to be a **channel region** 38. Further, a **source** electrode 37 is disposed over both the n(sup +)-type source **diffusion** layers 34 and the P-type base **diffusion** layer 33, and a P(sup +)-type drain layer 40 is formed above the high-resistance layer 32.

25/3,AB/8 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05576306
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 09-191106 [JP 9191106 A]
PUBLISHED: July 22, 1997 (19970722)
INVENTOR(s): FURUKAWA AKIO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-001804 [JP 961804]
FILED: January 09, 1996 (19960109)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **semiconductor** device in which the junctions between **diffusion** layers of source and drain can be made shallower and, at the same time, the resistances and capacitances of the junctions can be reduced and a method for manufacturing the device.

SOLUTION: In the element forming area of a silicon substrate 1 where an ordinary structure composed of a **channel** impurity layer 2, a gate insulating film 3, a **gate electrode** 4, side-wall insulating films 5, a shallow source 6, a shallow drain 7, a deep source 8, and a deep drain 9 is formed, pocket areas 10 having a conductivity opposite to that of the drains and containing an impurity at concentrations higher than that of the impurity in the **channel** impurity layer 2 are additionally formed under the gate end sections of the shallow source 6 and drain 7 so that parts of the areas 10 can come into contact with the bottoms of the source 6 and **drain** 7 and the **areas** 10 can be separated from the deep source 8 and drain 9. Therefore, parts of the source 6 and drain 7 are inverted into the opposite **conductivity** and shallow **junctions** are formed. In addition, the contacting areas of the pocket **areas** 10 with the **source** 6 and drain 7 in the depth direction become smaller.

25/3,AB/9 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

04671003
LATERAL CONDUCTIVITY MODULATION MOSFET

PUB. NO.: 06-342903 [JP 6342903 A]
PUBLISHED: December 13, 1994 (19941213)
INVENTOR(s): NAKAGAWA AKIO
YAMAGUCHI YOSHIHIRO
WATANABE KIMINORI
OHASHI HIROMICHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-108640 [JP 94108640]

FILED: May 23, 1994 (19940523)

ABSTRACT

PURPOSE: To obtain a **lateral conductivity** modulation MOSFET, in which a latch-up is difficult to be generated.

CONSTITUTION: A p-type base **diffusion** layer 33 is formed to a high resistance layer 32 section on the drain layer side of a **semiconductor** substrate wafer with an n- type high resistance layer 32 and a p(sup +) type drain layer 40 selectively formed onto the surface of the layer 32, and an n'' type source **diffusion** layer 34 is formed into the base **diffusion** layer 33. In a **lateral** type **conductivity** modulation type MOSFET, a **gate electrode** 36 is shaped onto a the base **diffusion** layer 33 as a **channel region** held by the **source diffusion** layer 34 and the high resistance layer 32 through a gate insulating film 35, and a source electrode 37 brought into contact with both the source **diffusion** layer 34 and the base **diffusion** layer 33 is formed. An opening section exposed onto the wafer surface of the high resistance layer 32 is formed in an insular shape completely surrounded by the base **diffusion** layer 33, and the drain layer 40 is shaped selectively to the surface of a p(sup +) type **diffusion** layer 39 formed on the surface of the high resistance layer 32.

25/3,AB/10 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

03663146
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 04-028246 [JP 4028246 A]
PUBLISHED: January 30, 1992 (19920130)
INVENTOR(s): NAGATOMO MASAO
SHIMANO HIROKI
OKUDAIRA TOMOHITO
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-132998 [JP 90132998]
FILED: May 23, 1990 (19900523)
JOURNAL: Section: E, Section Number 1200, Volume 16, Number 196, Pg. 75, May 12, 1992 (19920512)

ABSTRACT

PURPOSE: To improve the breakdown strengths of **junctions** between the second **conductivity** type high-concentration impurity regions of a MOS transistor and low- concentration first conductivity type impurity regions by a method wherein the low- concentration first conductivity type impurity regions are respectively formed between the second conductivity type high-concentration impurity regions and the first conductivity type high-**concentration channel** stop region of the MOS transistor.

CONSTITUTION: Arsenic ions 19 are ion-implanted in the surface of a silicon substrate 1 in the direction perpendicular to the substrate surface using a **gate electrode** 3 with a sidewall oxide film 17 formed thereon and a field oxide film 7 as masks and thereafter, an activation treatment is conducted. Thereby, high-concentration n(sup +) impurity regions 5a are formed and an LDD structure consisting of **source** and **drain regions** is completed. Low-concentration P(sup -) impurity regions 15

are respectively formed between a **channel** stop layer 8 and the regions 5a at the end parts of the film 7. When a reverse voltage is applied to junctions between these regions 15 and the regions 5a, the **spread** of depletion layers which are formed at the junction regions is increased, an electric field which is applied to the junction surfaces is relaxed and the breakdown strengths of the junctions can be improved.
? DS17-

```
Set     Items   Description
S17     35017   (VOLT? OR POTENTIAL)(3N)CONDITION?
S18      2876   S3 AND S4
S19       156   S18 AND S7
S20        88   S19 AND S12
S21        21   S20 AND S13
S22         1   S21 AND S14
S23        20   S21 NOT S22
S24        10   S23 AND S15
S25        10   RD (unique items)
? S S23 NOT S24
            20  S23
            10  S24
     S26    10  S23 NOT S24
? S S26 AND S16
            10  S26
        342326  S16
     S27     0  S26 AND S16
? RD S26
>>>Duplicate detection is not supported for File 350.
>>>Duplicate detection is not supported for File 347.
>>>Duplicate detection is not supported for File 344.
>>>Duplicate detection is not supported for File 371.

>>>Records from unsupported files will be retained in the RD set.
...completed examining records
     S28    10  RD S26 (unique items)
? TA
>>>No matching display code(s) found in file(s): 65

 28/3,AB/1     (Item 1 from file: 2)
DIALOG(R)File   2:INSPEC
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01848780   INSPEC Abstract Number: A82046143, B82025087
  Title: Equivalent circuit for ion implanted counterdoped layers as
determined by MOS admittance and crosstalk measurements
  Author(s): Bach, H.G.; Fahrner, W.R.; Braunig, D.
  Author Affiliation: Dept. of Data Processing & Electronics,
Hahn-Meitner-Inst. for Nuclear Res., Berlin, West Germany
  Journal: Physica Status Solidi A    vol.68, no.2    p.589-601
  Publication Date: 16 Dec. 1981  Country of Publication: East Germany
  CODEN: PSSABA  ISSN: 0031-8965
  Language: English
  Abstract: Counterdoping ion implantation of doses above 10/sup 11/ cm/sup
-2/ into MOS structures leads to the formation of a p-n junction close to
the SiO/sub 2/-Si-phase boundary. The hf-C(V) curves of this structure show
an additional frequency dispersion in the implanted layer
accumulation regime. This dispersion is caused by the two-dimensional
current propagation into the lateral channel and into the bulk of the
silicon across the p-n junction underneath the gate electrode.
The lateral current spread is described by an infinitely distributed
```

equivalent network. The voltage and current along its components are calculated for a linear geometry of finite dimensions. The model is checked by the measurement of the input accumulation admittance and the measurement of the complex dot-to-dot crosstalk voltage. Identical values of sheet resistance, junction capacitance and effective **junction conductance** are found for either method.
Subfile: A B

28/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010651855
WPI Acc No: 1996-148809/199615
XRPX Acc No: N96-125181
Semiconductor IC device with voltage surge protection - has P **channel** MOSFET and N **channel** MOSFET to conduct during negative and positive voltage surges to dissipate overvoltage
Patent Assignee: NIPPONDENSO CO LTD (NPDE)
Inventor: ASAI A; ENYA T; TSURUTA K
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8037284	A	19960206	JP 94169738	A	19940721	199615	B
US 5610426	A	19970311	US 95505819	A	19950721	199716	

Priority Applications (No Type Date): JP 94169738 A 19940721
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8037284	A		10	H01L-027/04	
US 5610426	A		14	H01L-023/62	

Abstract (Basic): JP 8037284 A
The IC device includes a CMOS inverter (2). A protection circuit (8) is arranged between input pad (7) and input of CMOS inverter. A P **channel** MOSFET (10) and an N **channel** MOSFET (11) are connected between input conduction line (12) to CMOS inverter and ground. Gate terminals of both MOSFETs are connected to the input conduction line. In case of surge voltage of negative polarity, the P **channel** MOSFET conducts. In case of surge voltage of positive polarity, the N **channel** MOSFET conducts.
ADVANTAGE - Provides protection against positive and negative surge voltages without use of large resistors, occupying small area.
Dwg.1/11
Abstract (Equivalent): US 5610426 A
A **semiconductor** integrated circuit device comprising:
a **semiconductor** substrate;
an insulating layer disposed on said **semiconductor** substrate;
a **semiconductor** layer disposed on said insulating layer;
a **semiconductor** integrated circuit formed on said **semiconductor** layer, said integrated circuit having a first connection and a second connection;
an external connection terminal connected to said first connection and which provides an external connection; and
a protective circuit which protects said **semiconductor** integrated circuit from excess positive and negative voltages from said external connection terminal, said protective circuit including
a first conductivity type first impurity **diffusion** layer in

said **semiconductor** layer, said first impurity **diffusion** layer being electrically connected to said second connection,

a first conductivity type second impurity **diffusion** layer, said second impurity **diffusion** layer being disposed in said **semiconductor** layer, said second impurity **diffusion** layer being connected electrically to said first connection,

a **gate electrode** formed on said **channel** region via a gate insulating layer, said **gate electrode** being electrically connected to said first connection, and

a second conductivity type third impurity **diffusion** layer disposed in said **semiconductor** layer, said third impurity **diffusion** layer being connected electrically to said second connection;

wherein said second conductivity type third impurity **diffusion** layer forms a PN **junction** with said first **conductivity** type second impurity **diffusion** layer via said second conductivity type **channel** region.

Dwg.1,10/1

1

28/3,AB/3 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

008262563

WPI Acc No: 1990-149564/199020

Related WPI Acc No: 1996-277156

XRAM Acc No: C90-065482

XRPX Acc No: N90-115922

Semiconductor device with MISFET connected to high resistance load - formed by resistor portion of conductive circuit layers

Patent Assignee: SEIKO EPSON CORP (SHIH); SEIKO EPSON CO LTD (SHIH)

Inventor: KIMURA M

Number of Countries: 006 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 368646	A	19900516	EP 89311581	A	19891109	199020	B
JP 2130854	A	19900518	JP 88284686	A	19881110	199026	
US 5107322	A	19920421	US 89410936	A	19890922	199219	
US 5349206	A	19940920	US 89410936	A	19890922	199437	
			US 92871871	A	19920420		
KR 9403376	B1	19940421	KR 8916011	A	19891106	199605	
EP 368646	B1	19970305				199714	
US 5691559	A	19971125	US 89410936	A	19890922	199802	
			US 92871871	A	19920420		
			US 94308777	A	19940919		
US 5818090	A	19981006	US 89410936	A	19890922	199847	
			US 92871871	A	19920420		
			US 94308777	A	19940919		
			US 97917515	A	19970826		

Priority Applications (No Type Date): JP 88284686 A 19881110

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 368646	A		13		
Designated States (Regional): FR GB NL					
US 5107322	A		11		
US 5349206	A		28	H01L-027/01	CIP of application US 89410936
					CIP of patent US 5107322

EP 368646 B1 E 12 H01L-027/11
Designated States (Regional): FR GB NL
US 5691559 A 25 H01L-027/02 CIP of application US 89410936
Cont of application US 92871871
CIP of patent US 5107322
Cont of patent US 5349206
US 5818090 A H01L-027/02 CIP of application US 89410936
Cont of application US 92871871
Cont of application US 94308777
CIP of patent US 5254870
Cont of patent US 5349206
Cont of patent US 5691559
KR 9403376 B1 H01L-023/52

Abstract (Basic): EP 368646 A
Semiconductor device includes at least one MISFET with a source electrode connected to a conductive layer extending over the MISFET to a position over the **gate electrode**. A second conductive layer is connected to the first over the **gate electrode** and extends in an opposite direction e.g. to a power supply. A main portion of the second conductive layer is highly resistive so as to form a high-resistance circuit load USE - The MISFET and resistor form part of a high resistivity load type SRAM device. (claimed) ADVANTAGE - The length of the resistor is increased in relation to overall cell length so that miniaturisation is readily achieved while retaining the high resistance of the resistor.
Dwg.1b/5
Abstract (Equivalent): EP 368646 B
A **semiconductor** device comprising at least one static memory cell having an area defined by an arrangement of parallel data lines (DL), intersected by a word line (WL) and a power supply line (VDD); each cell formed on a substrate (1) and including: at least one MISFET (Q3, Q4) having a source electrode, drain **electrode** and a gate **electrode** (4), the **gate electrode** being connected to the word line; a first circuit layer (13) spaced from said substrate by a first insulator (12) and connected to one of the source and drain electrodes (9) of the MISFET through a first contact **hole** (16); and a second circuit layer (15), having a high resistance load (R1, R2), which is connected to said first circuit layer by a second contact **hole** (18) and **spaced** therefrom by a second insulator (14), the high resistance load (R1, R2) being spaced from the substrate by at least the first and second insulators (12, 14), characterised in that the second contact **hole** (18) is disposed at least partially over the **gate electrode** (4) so that the second circuit layer extends from the second contact **hole** to the power supply line (VDD).
Dwg.1b/5
Abstract (Equivalent): US 5691559 A
Semiconductor device includes at least one MISFET with a source electrode connected to a conductive layer extending over the MISFET to a position over the **gate electrode**. A second conductive layer is connected to the first over the **gate electrode** and extends in an opposite direction e.g. to a power supply. A main portion of the second conductive layer is highly resistive so as to form a high-resistance circuit load USE - The MISFET and resistor form part of a high resistivity load type SRAM device. (claimed) ADVANTAGE - The length of the resistor is increased in relation to overall cell length so that miniaturisation is readily achieved while retaining the high resistance of the resistor.
Dwg.0/17B

US 5107322 A

Integrated circuit comprises interconnect means to extend the value of an integrated passive electrical component (I) coupled to other passive and active electrical elements (II) in the circuit, at least some of elements (II) including **diffusion** regions. The extended value is provided without any change in, or allowing for a reduction in the scale of integration among elements (II). The interconnect means comprises at least two conductor layers separated by an insulating layer, with a second of the conductive layers comprising component (I) formed in it for a substantial length of it. The first conductor layer provides electrical connection between the one element (II) and the second layer, and the second layer and the integrated component (I) have an extended **conductor** length extending **laterally** away from the second contact **hole**, in a second direction opposite to the first direction, over and insulated from the first contact **hole**. Component (I) in the second conductor layer is formed in spaced relation from the second contact **hole**, with the magnitude of component (I) being extended due to the addition of the extended conduits length. ADVANTAGE - Interconnect means is provided to extend values for integrated passive elements, e.g. resistances in an SRAM, while maintaining the desired integrated circuit scale.

28/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003024598
WPI Acc No: 1981-C4612D/198112
Semiconductor integrated circuit for e.g. wrist-watch - has two **junction** FETS one rendered **conductive** when gate voltage is equal to source voltage of other
Patent Assignee: DAINI SEIKOSHA KK (DASE)
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
GB 1586405	A	19810318				198112 B
US 4329700	A	19820511				198221
SG 8200448	A	19960705	SG 82448	A	19820911	199642

Priority Applications (No Type Date): JP 7751468 A 19770504
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SG 8200448	A				Previous Publ. patent GB 1586405

Abstract (Basic): GB 1586405 A

The **semiconductor** device comprises two junction FETs of opposite polarity. An input terminal is connected to **gate electrodes** of the transistors, and an output terminal to the drain electrodes. One transistor is rendered non-conductive when the gate voltage is equal to the source voltage, and is rendered conductive when the gate voltage is equal to the source voltage of the other transistor.

Pref. the **channel** of one transistor extends parallel to the surface of a substrate in which it is formed and the **channel** of the other transistor extends perpendicular to the surface of the substrate. Pref. the **diffusion** depth of the gate of one transistor is less than that of the source, and the **diffusion** depth of the drain of the other transistor is less than that of the gate.

28/3,AB/5 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07621737
LATERAL SUPERJUNCTION **SEMICONDUCTOR** DEVICE

PUB. NO.: 2003-115588 [JP 2003115588 A]
PUBLISHED: April 18, 2003 (20030418)
INVENTOR(s): KINZER DANIEL M
SRIDEVAN SRIKANT
APPLICANT(s): INTERNATL RECTIFIER CORP
APPL. NO.: 2002-186923 [JP 2002186923]
FILED: June 26, 2002 (20020626)
PRIORITY: 01 891727 [US 2001891727], US (United States of America), June 26, 2001 (20010626)

ABSTRACT
PROBLEM TO BE SOLVED: To provide a new **lateral conductive** type **superjunction** MOSFET device.

SOLUTION: Laterally extending **trenches** 20 to 23 are arranged at intervals in a P- region. An N- **diffusion** region is arranged along walls of **trenches** 20 to 23 so that the concentration and thickness of the N- **diffusion** region and a P- mesa are depleted fully during reverse blocking operation. The **MOS gate** structure is joined to one **edge** of the **trenches** 20 to 23 and the drain is connected to the other end of thereof. The other N- layer or the insulting oxide layer can be arranged between the P-- substrate 11 and the P- region 13.

28/3,AB/6 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06713622
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 2000-299457 [JP 2000299457 A]
PUBLISHED: October 24, 2000 (20001024)
INVENTOR(s): YAMAGUCHI KAZUMI
APPLICANT(s): NEC KANSAI LTD
APPL. NO.: 11-105126 [JP 99105126]
FILED: April 13, 1999 (19990413)

ABSTRACT
PROBLEM TO BE SOLVED: To provide a **semiconductor** device, having a bidirectional diode in which the waveform of its breakdown voltage is hard and the **dispersion** in manufacture of the breakdown voltage and the variation of the products are small.

SOLUTION: A bidirectional diode 34 of a p-**channel** power MOSFET, provided with a **gate electrode** 27 in a **groove** 23, has a **conductive** p-n **junction** structure in which a p-type polysilicon layer 36 is sandwiched between N+-type polysilicon layers 35. Ion implantation, which is performed for forming the polysilicon layer 36, is

performed before a polysilicon block is formed after coating the surface of a wafer with a polysilicon film, and in addition, the thermal **diffusion** performed after the ion implantation is performed simultaneously with the thermal **diffusion** which is performed for forming a base region 29, after the ion implantation. Moreover, the ion implantation and thermal **diffusion** which are formed for forming the N+-type polysilicon layers 35 are performed simultaneously with the ion implantation and thermal **diffusion**, which are performed for forming a contact base region 20a.

28/3,AB/7 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

05637316
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 09-252116 [JP 9252116 A]
PUBLISHED: September 22, 1997 (19970922)
INVENTOR(s): AOYAMA MASASHIGE
APPLICANT(s): SANYO ELECTRIC CO LTD [000188] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-057707 [JP 9657707]
FILED: March 14, 1996 (19960314)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce junction capacitance between a **gate electrode** and an impurity **diffusion** layer by separating the **gate electrode** and the **diffusion** layer by utilizing a **groove** formed to a substrate in a MOS transistor to be fined.

SOLUTION: In a **semiconductor** device, a **groove** is formed to a substrate 1 on the drain **diffusion** layer 24, 25 sides, and a side wall spacer is formed so as to bury the **groove**. A layer insulating film 26 consisting of a BPSG film is formed on the whole surface of the substrate, and contact **holes** are shaped onto an N(sup +) type source-drain **diffusion** layer 24 and a P(sup +) type source-drain **diffusion** layer 25. Barrier films 27 composed of a titanium film and a titanium nitride film and metal electrodes 28 made up of an aluminum film are formed. Through the contact **holes**. Accordingly, fining is **conducted, junction** capacitance between a polycide-**gate gate electrode** and the drain **diffusion** layer is reduced, the depth of the drain **diffusion** layers 24, 25 can be deepened, and a power- supply voltage can be maintained at approximately 5V in accordance with conventional devices.

28/3,AB/8 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

03646680
INSULATED GATE TYPE BIPOLAR TRANSISTOR

PUB. NO.: 04-011780 [JP 4011780 A]
PUBLISHED: January 16, 1992 (19920116)
INVENTOR(s): YAMAMOTO TAKESHI

OKABE NAOTO
TOKURA NORIHITO
APPLICANT(s): NIPPONDENSO CO LTD [000426] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-115578 [JP 90115578]
FILED: April 30, 1990 (19900430)
JOURNAL: Section: E, Section Number 1192, Volume 16, Number 162, Pg. 80, April 20, 1992 (19920420)

ABSTRACT

PURPOSE: To eliminate a latchup by controlling a first carrier electric resistance value by a source layer shape between a first contact and a **channel** region, and preventing **conduction** of a pn **junction.**

CONSTITUTION: A p(sup +) type silicon substrate is prepared, and an n(sup -) type layer of low impurity concentration **semiconductor** is formed by an epitaxial growth. A p(sup +) type drain layer 1, an n(sup -) type drain layer 2 are formed of the substrate and the n(sup -) type layer, and the surface of the layer 2 is oxidized to form a gate oxide film 3. A **gate electrode** 4 of a polysilicon film is formed thereon. With the electrode 4 as a mask boron is **diffused** to form a p-type base layer 5. Then, the center of the window of the electrode 4 is covered with a resist film patterned in a shape opened in a T shape, phosphorus ions are implanted to form an n(sup +) type source layer 6. Since carrier electric resistance value R(sub 1) is controlled by the shape of the layer 6 to prevent **conduction** of the pn **junction,** a source resistance is improved to prevent a latchup.

28/3,AB/9 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

02477767
SEMICONDUCTOR INTEGRATED CIRCUIT

PUB. NO.: 63-094667 [JP 63094667 A]
PUBLISHED: April 25, 1988 (19880425)
INVENTOR(s): TAKATSUKA ICHIRO
APPLICANT(s): FUJI ELECTRIC CO LTD [000523] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-239755 [JP 86239755]
FILED: October 08, 1986 (19861008)
JOURNAL: Section: E, Section Number 655, Volume 12, Number 330, Pg. 83, September 07, 1988 (19880907)

ABSTRACT

PURPOSE: To realize isolation between elements without employing an isolating **diffused** layer by a method wherein a depletion layer **spread** in a 2nd conductivity type layer directly below an electrode is brought into contact with a depletion layer produced by a p-n **junction** between a first **conductivity** type substrate and the 2nd conductivity type layer.

CONSTITUTION: A p-type epitaxial layer 2 is formed on an n-type silicon substrate 1 by epitaxial growth and further a silicon oxide film 3 is laminated on the epitaxial layer 2 and an Al electrode 4 is formed on a part of the oxide film 3. A **channel**-doped type p-type MOS FET is formed by providing an Al **gate electrode** 6 on the p-type epitaxial layer 2 with the oxide film 3 between. Even if the p-type layer 2 and the substrate 1 are made to be equipotential by grounding the electrode

4, a depletion layer 52 produced by the electrode 4 is contacted with a depletion layer 51 produced by the p-n junction between the epitaxial layer 2 and the substrate 1 to form an element isolation layer 5. As a depletion layer 53 produced directly below the **gate electrode** 6 is also contacted with the depletion layer 51 of the p-n junction between the n-type substrate 1 and the p-type layer 2, a source 71 and a drain 72 are electrically separated from each other. Therefore, this FET is of normally-OFF type.

28/3,AB/10 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

02230859
MANUFACTURE OF **SEMICONDUCTOR** DEVICE

PUB. NO.: 62-147759 [JP 62147759 A]
PUBLISHED: July 01, 1987 (19870701)
INVENTOR(s): SAITO RYUICHI
MONMA NAOHIRO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-287750 [JP 85287750]
FILED: December 23, 1985 (19851223)
JOURNAL: Section: E, Section Number 564, Volume 11, Number 382, Pg. 123, December 12, 1987 (19871212)

ABSTRACT

PURPOSE: To sufficiently lower the **lateral diffusion** of **conductive** impurity in the polysilicon and make small fluctuation due to small size and high yield by including one element among oxygen, nitrogen and carbon into the entire part of polysilicon.

CONSTITUTION: An insulation film 2 is deposited on a **semiconductor** substrate 1, the polysilicon layer 3 is futher deposited and it is etched like islands. Next, the oxygen ion 4, for example, is introduced into the polysilicon 3 by the ion implantation method, a gate insulation film 5 is formed, an electrode 9 is then formed, and the conductive impurity ion 8 is introduced by the ion implantation method to form a **diffused** layer 6 which becomes the source and drain. An insulation film 10 is then deposited and the heat processing is carried out. In this case, the **lateral diffusion** of **conductive** impurity is suppressed in the **diffusion** layer 6 due to existence of oxygen and the **diffusion** layer 6 is not connected even when the **gate electrode** 9 has the width of 2μm or less. Thereafter, a contact **hole** is formed on the insulation film 10, the Al electrode 11 is then formed, thus completing small size polysilicon MOS transistor element.

31/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7412072 INSPEC Abstract Number: B2002-11-2560L-002
Title: A new **lateral conductivity** modulated thyristor with current saturation and low turn-off time
Author(s): You-Sang Lee; Soo-Seung Kim; Jae-Keun Oh; Yearn-Ik Choi; Min-Koo Han
Author Affiliation: Sch. of Electr. English, Seoul Nat. University, South Korea
Conference Title: Proceedings of the 14th International Symposium on Power Semiconductor Devices and ICs (Cat. No.02CH37306) p.113-16
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xx+311 pp.
ISBN: 0 7803 7318 9 Material Identity Number: XX-2002-01938
U.S. Copyright Clearance Center Code: 0-7803-7318-9/02/$17.00
Conference Title: Proceedings of the 14th International Symposium on Power Semiconductor Devices and ICs
Conference Sponsor: IEEE Electron Devices Society; Inst. Electr. English Japan
Conference Date: 4-7 June 2002 Conference Location: Sante Fe, NM, USA
Language: English
Abstract: A new **MOS-gate** controlled thyristor, entitled **lateral conductivity** modulated thyristor (LCMT), which exhibits a high current saturation and a low turn-off time, is proposed and successfully fabricated. Experimental results show that the new LCMT achieves a current saturation capability larger than 1200 A/cm/sup 2/ even at high anode voltages. The forward voltage drop of LCMT is 1.2 V at 100 A/cm/sup 2/ where 10 V was biased to the dual gates. The turn-off time of LCMT without any lifetime-control process is 1.5 mu s while that of LCMT without p+ diverter is about 2.9 mu s. The p+ diverter successfully diverts **holes** in the drift region during the turn-off. The LCMT, where any trouble-some parasitic thyristor mechanism is eliminated, completely suppresses a latch-up and increases the maximum controllable current considerably. The proposed LCMT showed excellent current saturation characteristics at an elevated temperature and exhibited a negative temperature coefficient in high saturation current density.
Subfile: B

31/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7321348 INSPEC Abstract Number: B2002-08-2560L-002
Title: A new **lateral conductivity** modulated thyristor (LCMT)
Author(s): Lee, Y.S.; Han, M.K.; Choi, Y.I.
Author Affiliation: Sch. of Electr. English, Seoul Nat. University, South Korea
Conference Title: 2001 International Semiconductor Device Research Symposium. Symposium Proceedings (Cat. No.01EX497) p.145-7
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA xiv+669 pp.
ISBN: 0 7803 7432 0 Material Identity Number: XX-2002-00451
Conference Title: 2001 International Semiconductor Device Research Symposium. Symposium Proceedings
Conference Sponsor: IEEE; Electron Devices Society; Army Res. Office; NSF; Army Res. Laboratory; NASA; Electr. & Comput. English Dept.; University Maryland
Conference Date: 5-7 Dec. 2001 Conference Location: Washington, DC, USA
Language: English

Abstract: The purpose of our work is to report a new lateral **MOS-gated** thyristor, named LCMT, with increased safe operating area (SOA) and decreased turn-off characteristics. In the proposed LCMT, the SOA is improved due to increased current saturation capability by elimination of the parasitic thyristor. The turn-off time is decreased by employing a p+ diverter which successfully diverts **holes** during the turn-off process. Our experimental results show that the LCMT also exhibits positive-temperature characteristics. We compare the results for the LCMT with those of the widely used LIGBT (lateral insulated gate bipolar transistor).

Subfile: B

31/3,AB/3 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

16510931 PASCAL Number: 04-0156406

A new **lateral conductivity** modulated thyristor with current saturation and low turn-off time

ISPSD '02 : 14th international symposium on power **semiconductor** devices & ICS : Santa FE NM, 4-7 June 2002

LEE You-Sang; KIM Soo-Seung; OH Jae-Keun; CHOI Yearn-Ik; HAN Min-Koo

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IEEE Electron Devices Society, United States; Institute of Electrical ENgineers of Japan, Japan

International symposium on power semiconductor devices & ICS, 14 (Santa FA NM USA) 2002-06-04

2002 113-116

Publisher: IEEE, Piscataway NJ

Language: English

A new **MOS-gate** controlled thyristor, entitled **lateral conductivity** modulated thyristor (LCMT), which exhibits a high current saturation and a low turn-off time, is proposed and successfully fabricated. Experimental results show that the new LCMT achieves a current saturation capability larger than 1200A/cm SUP 2 even at high anode voltages. The forward voltage drop of LCMT is 1.2V at 100A/cm SUP 2 where 10V was biased to the dual gates. The turn-off time of LCMT without any lifetime-control process is 1.5 mu s while that of LCMT without p+ diverter is about 2.9 mu s. The p+ diverter successfully diverts **holes** in the drift region during the turn-offThe LCMT, where any trouble-some parasitic thyristor mechanism is eliminated, completely suppresses a latch-up and increases the maximum controllable current considerably. The proposed LCMT showed excellent current saturation characteristics at an elevated temperature and exhibited a negative temperature coefficient in high saturation current density.

31/3,AB/4 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011372426
WPI Acc No: 1997-350333/199732

XRPX Acc No: N97-290400

Power insulated gate bipolar transistor device - has very deep increased concentration region between spaced bases of transistor and lifetime killing radiation dose applied to wafer

Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: KINZER D M

Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5644148	A	19970701	US 92945106	A	19920915	199732 B
			US 94364514	A	19941227	
			US 95461509	A	19950605	
			US 96674982	A	19960703	
IT 1272567	B	19970623	IT 93MI1898	A	19930903	199811

Priority Applications (No Type Date): US 92945106 A 19920915; US 94364514 A 19941227; US 95461509 A 19950605; US 96674982 A 19960703
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5644148	A		21	H01L-029/74	Cont of application US 92945106
					Cont of application US 94364514
					Cont of application US 95461509
IT 1272567	B			H01L-000/00	

Abstract (Basic): US 5644148 A

The power transistor device has bipolar device forward current carrying characteristics and **MOS gate** control characteristics. The device includes a substrate (300) and a layer of **semiconductor** material (301) positioned on the substrate. The **semiconductor** material is of a first conductivity type and is lightly doped and has an upper surface. At least two spaced base regions (310,311) of opposite conductivity type extend into the upper surface of the layer of **semiconductor** material of first conductivity type to a given depth. At least two source regions (312,313) of the first conductivity type are formed in respective spaced base regions and define at least one surface **channel** region between them. A gate insulation layer (315) is positioned over the **channel** region. A conductive gate layer (113) is positioned over the gate insulation layer. A first main electrode is connected to the source regions. A further region of conductivity type opposite the first conductivity type extends into the upper surface of the **semiconductor** material of first **conductivity** type and spaced **lateral** distance away from the spaced base regions.

A second main electrode is connected to the further region of opposite conductivity type. The region between the spaced base regions includes an increased conductivity region with an increased concentration of carriers of the first conductivity type which extends from the upper surface of the **semiconductor** material to a depth greater than the depth of the spaced base regions. The increased concentration is greater than that of the remaining portion of the layer of **semiconductor** material over the full depth of the increased concentration region and is greater than twice that of the remaining portion of the layer of **semiconductor** material in a portion of the increased conductivity region that is adjacent of the upper surface.

ADVANTAGE - Increases speed at which transistor may be switched by increasing space between base regions forming junction pattern.

Dwg.22/22

34/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010150098
WPI Acc No: 1995-051350/199507
XRPX Acc No: N95-040365
Lateral SOI device for HV and power, with high breakdown voltage - has lateral drift region on buried insulating layer with drift region of wide band-gap **semiconductor** material e.g. silicon carbide having linearly graded doping profile
Patent Assignee: PHILIPS ELECTRONICS NV (PHIG); KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS ELECTRONICS NORTH AMERICA CORP (PHIG)
Inventor: PEIN H; PEIN H B
Number of Countries: 008 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5378912	A	19950103	US 93151075	A	19931110	199507 B
EP 652599	A1	19950510	EP 94203200	A	19941103	199523
JP 7183522	A	19950721	JP 94272454	A	19941107	199538
EP 652599	B1	19970521	EP 94203200	A	19941103	199725
DE 69403306	E	19970626	DE 603306	A	19941103	199731
			EP 94203200	A	19941103	
KR 359712	B	20030124	KR 9429224	A	19941109	200339

Priority Applications (No Type Date): US 93151075 A 19931110
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5378912	A		5	H01L-029/10	
EP 652599	A1	E	6	H01L-029/772	
Designated States (Regional): DE FR GB IT NL					
JP 7183522	A		5	H01L-029/786	
EP 652599	B1	E	7	H01L-029/24	
Designated States (Regional): DE FR GB IT NL					
DE 69403306	E			H01L-029/24	Based on patent EP 652599
KR 359712	B			H01L-021/30	Previous Publ. patent KR 95015611

Abstract (Basic): US 5378912 A
The lateral SOI device includes a buried insulating layer on a substrate, and a lateral **semiconductor** device e.g. an LDMOS transistor. The **semiconductor** device includes a source, a **channel**, an insulated **gate electrode** over the **channel**, and a lateral drift region on the buried insulating layer, with a linearly graded lateral doping profile. A drain is laterally **spaced** apart from the **channel** and connected to the **channel** region by the drift region.
The lateral drift region is formed of a wide bandgap **semiconductor** material, having a wider bandgap than that of silicon pref. silicon carbide. Pref. the drain, source and part of the **channel** are in a **semiconductor** layer over the drift region. The drift region thickness is pref. between about 0.05 micron and 2.0 microns.
USE/ADVANTAGE - E.g. lateral IGBT, lateral thyristor, or lateral HV diode on insulating layer. Reduced on-resistance; good thermal conductivity and dielectric constant characteristics; commercially mfd. with silicon processing.
Dwg.2/3
Abstract (Equivalent): EP 652599 B
A lateral **Semiconductor**-on-Insulator (SOI) device comprising a substrate, a buried insulating layer on the substrate, and a lateral **semiconductor** device on the insulating layer, the

semiconductor device comprising a source region of a first conductivity type, a **channel** region of a second conductivity type opposite to that of the first, an insulated **gate electrode** over the **channel** region, a lateral drift region of the first conductivity type on the buried insulating layer, and a drain region of the first **conductivity** type, **laterally spaced** apart from the **channel** region and connected thereto by the drift region, characterised in that a portion of the **semiconductor** device comprising at least the drain region is made in a first **semiconductor** material and that the drain region is provided in a layer of the first **semiconductor** material provided on top of the drift region, where the lateral drift region is formed of a second **semiconductor** material having a bandgap larger than that of the first **semiconductor** material which is silicon, germanium or a combination of both.

Dwg.1/3

34/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004485138
WPI Acc No: 1985-312016/198550
XRPX Acc No: N85-231668

Isolated bidirectional power MOSFET - has conduction **channel** induced **laterally** through **vertical** isolation region during ON state of FET

Patent Assignee: EATON CORP (EAYT)
Inventor: BENJAMIN J A; LADE R W; SCHUTTEN H P
Number of Countries: 005 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 164094	A	19851211				198550	B
JP 61046070	A	19860306				198616	

Priority Applications (No Type Date): US 84618442 A 19840608
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 164094	A	E	12		

Designated States (Regional): DE FR GB NL

Abstract (Basic): EP 164094 A

Two electrodes respectively connected to two **semiconductor** regions, are also connectable in an AC load line. A potential biases a **gate electrode** so as to apply an electric field and induce a conduction **channel** through an isolation region between the two regions during each half cycle of the AC line. During one half cycle, current flows from one to the other electrode via a conduction **channel**. During a second half cycle, the current flow is reversed.

The isolation region (6) of **semiconductor** material is vertically-arranged and provides blocking in an OFF state. The conduction **channel** (16) is formed horizontally through the isolation region when the FET is in an ON state.

USE/ADVANTAGE - Bidirectional AC power switching, enchances AC blocking capability.

1/4

34/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003961626
WPI Acc No: 1984-107170/198417
XRAM Acc No: C84-045550
XRPX Acc No: N84-079602
FET with planar doped barrier gate - including tow undoped planar regions and two oppositely doped planar regions
Patent Assignee: US SEC OF ARMY (USSA)
Inventor: AUCOIN T R; MALIK R J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4442445	A	19840410	US 81323858	A	19811123	198417	B

Priority Applications (No Type Date): US 81323858 A 19811123
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4442445	A		6		

Abstract (Basic): US 4442445 A
3-Terminal epitaxial layer FET comprises (a) a **semiconductor** substrate (10) having a first type planar **channel** region (16) formed on it, operating as a **lateral conductive channel** for charge carriers associated with the conductivity type; (b) first and second spaced terminals (18, 20) serving as source and drain electrodes on the **channel** region; and (c) a control terminal (22) between the first and second terminals for controlling lateral flow of charge carriers between them, including a gate having (i) a pair of undoped planar regions (30, 28) one contiguous with the **channel** region; (ii) a thin, highly doped opposite type planar region (26) between the undoped regions; and (iii) an outer highly doped first type planar planar region (32) on the other undoped region; and (iv) a **gate electrode** (24) on the outer region, **vertically spaced** from the **channel** region.
In a pref. embodiment, a buffer layer (14, 44) is provided between the substrate and the **channel** region. The substrate (10) is pref. a III-V cpd., especially GaAs.
The structure provides control over barrier height and reverse voltage characteristics, and provides highly output power than with Schottky barrier gates. The buffer layer improves confinement and reduces noise.
1,2/4

34/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003549317
WPI Acc No: 1982-97314E/198245
Related WPI Acc No: 1993-143111
Semiconductor device mfr. with electrode having insulator on sidewalls - pref. for **gate electrodes** and/or multilevel conductors
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: FU H S; TASCH A F; CHATTERJEE P K; FU H
Number of Countries: 001 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4356040	A	19821026				198245 B
US 4356040	B	19911210				199201
US 5393690	A	19950228	US 80146938	A	19800502	199514
			US 81276324	A	19810622	
			US 84657456	A	19841003	
			US 85739751	A	19850531	
			US 86928715	A	19861110	
			US 88178827	A	19880405	
			US 90614546	A	19901219	
			US 92933606	A	19920821	
			US 936864	A	19930121	

Priority Applications (No Type Date): US 80146938 A 19800502; US 81276324 A 19810622; US 84657456 A 19841003; US 85739751 A 19850531; US 86928715 A 19861110; US 88178827 A 19880405; US 90614546 A 19901219; US 92933606 A 19920821; US 936864 A 19930121

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4356040	A		14		
US 5393690	A		14	H01L-021/70	Div ex application US 80146938
					Cont of application US 81276324
					Cont of application US 84657456
					Cont of application US 85739751
					Cont of application US 86928715
					Cont of application US 88178827
					Cont of application US 90614546
					Cont of application US 92933606
					Div ex patent US 4356040
					Cont of patent US 5202574

Abstract (Basic): US 4356040 A

A device is mfd. including (a) forming a conductive layer on a substrate; (b) patterning to form at least one electrode (116) having a top surface and sidewalls; (c) forming a conformal insulating layer over the electrode; and (d) anisotropically removing insulator except from electrode sidewalls (118a).

In a first embodiment, useful for multilevel conductors, the substrate is **semiconducting** having a thin insulating layer on its surface. An insulator layer is deposited between (a) and (b), and patterned with the electrode, so conductor and insulator have coplanar **vertical edges**. A subsequently deposited **conductor** is **laterally** spaced from the electrode by the sidewalls.

In a further embodiment, with substrate as (I), and (b) forming a **gate electrode**, (d) is followed by (e) ion implanting impurities using electrode and sidewall insulator as mask, forming doped regions (120, 122) laterally spaced from the **gate electrode**.

The sidewall insulation reduces inter level shorts, reduces **gate** overlap, protects **gate electrode edges** during processing and reduces birds break formation during subsequent thermal oxidation of the substrate.

Abstract (Equivalent): US 5393690 A

A method is claimed for making a **semiconductor** charge-coupled device (CCD), comprising:

a) forming a first conductor of poly-Si over a **semiconductor** substrate;

b) forming an insulating layer, less than 1000 angstrom thick, between the first conductor and the substrate;

c) forming a sidewall insulator of SiO2 on a sidewall of the first conductor, wherein the sidewall insulator is at least 1000 angstrom thick and is at least 1.4 times as thick as the insulating layer;

d) forming a second **conductor** of poly-Si **laterally** adjacent to the first conductor and abutting the sidewall insulator;

e) forming an essentially uniform region of modified surface potential, whereby no perturbation impedes transfer of charge in the device.

USE - Useful in mfr. of **semiconductor** devices to provide improved insulation between interlevel conducting layers.

ADVANTAGE - In devices requiring multiple-level poly-Si electrodes. Shorts between electrodes are reduced. In MOS devices, operating parameters are improved.

Dwg.8/9

39/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011444693
WPI Acc No: 1997-422600/199739
XRPX Acc No: N97-352088
Semiconductor device mfg method e.g. for MOSFET - involves forming shallow junction layers and deep **junction** layer of different **conductivity** type on silicon substrate
Patent Assignee: NEC CORP (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9191106	A	19970722	JP 961804	A	19960109	199739	B

Priority Applications (No Type Date): JP 961804 A 19960109
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9191106	A		10		

Abstract (Basic): JP 9191106 A
The method involves forming a **channel** impurity layer (2) over an element formation area of a silicon substrate (1). Above the **channel**, a gate insulating film (3) and a **gate electrode** (4) are formed, sequentially. A side attachment wall insulating film (5), a shallow source (6), a shallow drain (7), a deep source (8) and a deep drain (9) are also formed in the silicon substrate, selectively. A pocket area (10) is formed in the shallow source and in the shallow drain of the **channel** impurity layer.
The conductivity type of the pocket area is opposite to that of the shallow drain. The impurity concentration of the pocket area is higher than the impurity **concentration** of the **channel** impurity layer. The **deep** source and deep drain are mutually separated. The shallow source and shallow drain are comprised by mutually opposite conductive type **semiconductors**.
ADVANTAGE - Reduces contact area of pocket area contacting source and drain. Achieves size reduction. Improves short **channel** effect and switching velocity.
Dwg.1/7

39/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010040587
WPI Acc No: 1994-308298/199438
XRAM Acc No: C94-140585
XRPX Acc No: N94-242503
Structure of FET - incorporates **channel** layer whose forbidden energy gap increases along its width and it is 1.1 ev at junction of this layer and buffer layer
Patent Assignee: NEC CORP (NIDE)
Inventor: KUZUHARA M; ONDA K
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6236898	A	19940823	JP 934473	A	19930114	199438	B
US 5596211	A	19970121	US 94181029	A	19940114	199710	

US 95544724 A 19951018

Priority Applications (No Type Date): JP 934473 A 19930114
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6236898	A		7	H01L-021/338	
US 5596211	A		10	H01L-035/26	Cont of application US 94181029

Abstract (Basic): JP 6236898 A

The structure of FET is obtained by depositing a buffer layer (2) made of In, 0.52 Al and 0.48 As, over a **semiconductor** InP wafer (1). Over this layer, a **channel** layer (3) made up of In (1-x) Gax Asy P (1-y) composition is formed. A spacer layer (4) of In,0.52 Al and 0.48 As composition is deposited over this **channel** layer. An epitaxial layer (7) having In,0.53 Ga and 0.47 As composition is formed on a conductive layer (5) made of In, 0.52 Al and 0.48 As composition, which inturn is placed on a spacer layer.

In between the epitaxial layer and the **conductive** layer, a schottky **junction** layer (6) of In,0.52 Al and 0.48 As composition is placed. A **gate electrode** (10) is formed at the center of the epitaxial layer by etching a portion of this layer. The source and drain electrodes (8,9) are formed on either side of the **gate electrode**. The forbidden energy gap of the grey coloured **channel** layer increases from 0.9 ev to 1.1 ev, along its width portion as it reaches the buffer layer.

ADVANTAGE -Enhances pressure withstanding capacity. Increases emission of secondary electrons.

Dwg.1/4

Abstract (Equivalent): US 5596211 A

A two-dimensional electron gas field effect transistor comprising a buffer layer, a **channel** layer, an N-type electron supply layer and a Schottky layer formed on a semi-insulating InP substrate in the named order, a **gate electrode** being formed in Schottky contact with the Schottky layer, a source electrode and a drain electrode being formed in ohmic contact with cap layers which are formed on the Schottky layer so as to put the **gate electrode** between them and apart from it, the **channel** layer being formed of an In1-xGaxAsyP1-y layer, where the values of ''x'' and ''y'' change in a **depth** direction of the **channel** layer so as to cause predetermined variation of energy gap value relative to **channel depth**, and where the values of x and y are selected to satisfy the relation x=(0.453y)(1+0.031y)

whereby lattice matching of the **channel** layer to the InP substrate is maintained throughout the **thickness** of the **channel** layer.

Dwg.1a/4

48/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5686154 INSPEC Abstract Number: B9710-2560H-019
Title: Macroscopic and microscopic studies of electrical properties of very thin silicon dioxide subject to electrical stress
Author(s): Daniel, E.S.; Jones, J.T.; Marsh, O.J.; McGill, T.C.
Author Affiliation: Thomas J. Watson Laboratory of Appl. Phys., California Inst. of Technol., Pasadena, CA, USA
Journal: Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures) Conference Title: J. Vac. Sci. Technol. B, Microelectron. Nanometer Struct. (USA) vol.15, no.4 p.1089-96
Publisher: AIP for American Vacuum Soc,
Publication Date: July-Aug. 1997 Country of Publication: USA
CODEN: JVTBD9 ISSN: 0734-211X
SICI: 0734-211X(199707/08)15:4L.1089:MMSE;1-P
Material Identity Number: C067-97009
U.S. Copyright Clearance Center Code: 0734-211X/97/15(4)/1089/8/$10.00
Conference Title: 24th Conference on the Physics and Chemistry of Semiconductor Interfaces
Conference Date: 12-15 Jan. 1997 Conference Location: Research Triangle Park, NC, USA
Language: English
Abstract: The electrical characteristics of various size tunnel switch diode devices, composed of Al/SiO/sub 2//n-Si/p/sup +/-Si layers, which operate with a range of parameters (such as current densities in excess of 10/sup 4/ A/cm/sup 2/) that stress the oxide layer far beyond the levels used in typical thin oxide metal-oxide **semiconductor** research have been examined. It is found that the first time a large current and electric field are applied to the device, a "forming" process enhances transport through the oxide in the vicinity of the **edges** of the **gate electrode** , but the oxide still retains its integrity as a tunnel barrier. The device operation is relatively stable to stresses of greater than 10/sup 7/ C/cm/sup 2/ areally averaged, time-integrated charge injection. Duplication and characterization of these modified oxide tunneling properties was attempted using scanning tunneling microscopy (STM) to stress and probe the oxide. Electrical stressing with the STM tip creates regions of reduced conductivity, possibly resulting from trapped charge in the oxide. **Lateral** variations in the **conductivity** of the unstressed oxide over regions roughly 20-50 nm across were also found.
Subfile: B

48/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015209676
WPI Acc No: 2003-270212/200327
XRPX Acc No: N03-214400
Image sensor device for image processing applications, has **semiconducting** substrate of first conductivity type, dielectric, buried **channel** of second **conductivity** type, and **lateral** overflow drain region of second conductivity type.
Patent Assignee: EASTMAN KODAK CO (EAST)
Inventor: BANGHART E K; STEVENS E G
Number of Countries: 032 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1289020	A2	20030305	EP 200278413	A	20020819	200327	B
JP 2003086782	A	20030320	JP 2002240045	A	20020821	200330	
US 20030042510	A1	20030306	US 2001945034	A	20010831	200331	
US 6624453	B2	20030923	US 2001945034	A	20010831	200364	

Priority Applications (No Type Date): US 2001945034 A 20010831
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1289020	A2	E	7	H01L-027/148	
	Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR				
JP 2003086782	A		5	H01L-027/148	
US 20030042510	A1			H01L-027/148	
US 6624453	B2			H01L-031/062	

Abstract (Basic): EP 1289020 A2
Abstract (Basic):

NOVELTY - The image sensor has a **semiconductor** substrate of a first conductivity type. There is a dielectric with a first thin portion and a second thick portion. There is a buried **channel** of the second conductivity type within the substrate, which spans the first thin portion. There is a lateral overflow drain region of the second conductivity type.

DETAILED DESCRIPTION - The lateral overflow drain region is located to span a portion of the second thick portion, for collecting excess photogenerated charges, to prevent blooming. There is also a **channel** stop, of the first conductivity type, which is positioned adjacent to the lateral overflow drain. A barrier region is located adjacent to the lateral overflow drain. The image sensor also includes a **gate electrode** covering the thin and thick portions.

USE - For image processing.

ADVANTAGE - The sensor has an anti-blooming structure, and provides for collection of excess photogenerated charges.

DESCRIPTION OF DRAWING(S) - The figure shows a vertical cross sectional view of the charge coupled device and the anti-blooming structure

Lateral overflow drain anti-blooming structure (10)
P type substrate (20)
N type buried channels (30)
Barriers (40)
Dielectric (50)
Lateral overflow drain (60)
Channel stop (70)
Active area dielectric (80)
Thick field dielectric (90)
pp; 7 DwgNo 3/3

48/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014626012
WPI Acc No: 2002-446716/200248
XRPX Acc No: N02-551356
Integrated **semiconductor** device has additional regions of high impurity concentration formed from front surface of chip upto N+ region formed in P-region
Patent Assignee: STMICROELECTRONICS SRL (SGSA)

Inventor: PATTI D
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
IT 1309699	B	20020130	IT 99MI331	A	19990218	200248	B
US 6441446	B1	20020827	US 2000505461	A	20000218	200276	

Priority Applications (No Type Date): IT 99MI331 A 19990218
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
IT 1309699	B			H01L-000/00	
US 6441446	B1		8	H01L-029/76	

Abstract (Basic): US 6441446 B1
Abstract (Basic):

NOVELTY - A bipolar transistor and a MOSFET are connected in an emitter switching configuration. The additional N+ region (17) of high concentration extends from the front surface of the chip upto the N+ region (14) formed in the P-region (13). The source and drain regions are subdivided by the N+ regions (26b,17b), forming channels between the N+ regions. Electrically conductive material (22b) is arranged over the **channel** to form a **gate electrode** of the MOSFET.

USE - For monolithic integrated **semiconductor** structures.

ADVANTAGE - Provides **semiconductor** device with integrated bipolar and MOSFET transistors in emitter switching configuration which has a lower resistance. The MOSFET transistor has **lateral conduction** and resistance between source and drain which are based on resistivity and dimensions of the **channel**. Avoids the additional processing steps for producing the **semiconductor** device in the emitter switching configuration.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the **semiconductor** device.

P-region (13)
N+ region (14)
Additional N+ region (17)
N+ region dividing drain region (17b)
Conductive material (22b)
N+ region dividing source region (26b)
pp; 8 DwgNo 4/4

48/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013788765
WPI Acc No: 2001-272976/200128
XRAM Acc No: C01-082697
XRPX Acc No: N01-194967
Self-aligned dual damascene fabrication for integrated circuits (ICs) using a number of etch stop layers and etching processes
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: LIU J; TSAI C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6211063	B1	20010403	US 99318020	A	19990525	200128	B

Priority Applications (No Type Date): US 99318020 A 19990525
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6211063	B1		12	H01L-021/4763	

Abstract (Basic): US 6211063 B1

Abstract (Basic):

NOVELTY - Fabrication comprises:

(1) depositing a 1st etch stop layer on a **semiconductor** substrate;

(2) depositing a silicate glass layer (35) over the etch stop layer;

(3) depositing a 2nd etch stop layer over the glass layer;

(4) patterning the 2nd etch stop layer to expose the top of silicate glass layer;

(5) depositing a hydrogen silsesquioxane (HSE) layer (46) over the 2nd etch stop layer and exposed silicate glass layer;

(6) depositing an oxide layer (48);

(7) patterning the oxide and hydrogen silsesquioxane layers by reactive ion etching using nitrogen gas to form upper **trenches**; and

(8) etching away silicate glass layer where not covered by 2nd etch stop layer using reactive ion etching not including nitrogen to form lower **trenches**.

The lower and overlying upper **trenches** form dual damascene structures.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for the formation of self-aligned dual damascene vias in the fabrication of an IC comprising providing 1st metal conductive traces through an insulating layer on a **semiconductor** substrate and carrying out the process above such that the lower **trenches** overlie the **conductive** traces and have **lateral** widths of 0.3-0.5 microns, and the formed upper **trenches** have lateral widths of 0.4-0.5 microns and overlie the lower **trenches**. The process further comprises after etching of silicate glass layer, etching of the 1st etch stop layer to reveal the top surfaces of the metal conductive traces and complete the self-aligned dual damascene vias, depositing a 2nd metal layer filling the lower and upper **trenches** and contacting the conductive traces, and etching back the 2nd metal layer to remove excess metal above the top surface of the oxide layer to complete the fabrication of the IC device.

A further INDEPENDENT CLAIM is included for the formation of self-aligned dual damascene vias in IC fabrication using the process above where the etch stop layers are silicon oxynitride layers.

USE - Fabrication of self-aligned dual damascene structures in the manufacture of integrated circuits (ICs).

ADVANTAGE - The problems of HSQ etch stop and HSQ etch profile bowing are eliminated

DESCRIPTION OF DRAWING(S) - The diagram shows a cross-section of a self-aligned dual damascene via.

Substrate (30)
1st metal layer (32)
Silicon oxide layer (34)
Silicate glass (35)
Fluorinated silicate glass layer (36)
Silicon oxynitride layer (38)
Hydrogen silsesquioxane layer (46)
Plasma enhanced silicon dioxide (48)
Passivation layer (56,62)
2nd metal layer (60)
pp; 12 DwgNo 12/12

48/3,AB/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012813513
WPI Acc No: 1999-619744/199953
XRPX Acc No: N99-457033
Bidirectional lateral insulated gate bipolar transistor (IGBT)
Patent Assignee: ALLEN BRADLEY CO LLC (ALLB)
Inventor: LI H P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5977569	A	19991102	US 96718842	A	19960924	199953 B
			US 97924106	A	19970905	

Priority Applications (No Type Date): US 97924106 A 19970905; US 96718842 A 19960924
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5977569	A		18	H01L-029/74	CIP of application US 96718842 CIP of patent US 5793064

Abstract (Basic): US 5977569 A
Abstract (Basic):

NOVELTY - The IGBT (100) is symmetrical and has an n-type drift region (160) in contact with an oxide layer (170). A p-type region (177) is provided above the drift region. The IGBT relies on a double RESURF structure which can be provided by a buried oxide layer, a floating doped region, or a horizontal PN junction.

DETAILED DESCRIPTION - The drift region is disposed above a **semiconductor** substrate (150). The drift region has a first end, a second end, and a middle section. A buried oxide layer is disposed between the substrate and the drift region as a RESURF structure. A p-type emitter/collector region is disposed above the first end of the drift region and has a first portion which is more heavily doped than a second portion. A p-type collector/emitter region is disposed above the second end of the drift region and has a first portion which is more heavily doped than a second portion. A first n-type region is disposed above the emitter/collector region. A second n-type region is disposed above the collector/emitter region. A gate oxide layer is disposed above the middle section of the drift region. An emitter/collector contact (102) is coupled to the first region and the emitter/collector region. A collector/emitter contact (104) is coupled to the second region and the collector/emitter region. The drift region includes a **channel** area for **laterally conducting** a current between the collector/emitter contact and the emitter/collector contact. A first **gate electrode** is coupled to the gate oxide layer and is disposed above the first region. A second **gate electrode** is coupled to the gate oxide layer and is disposed above the second region. A doped region is disposed between the gate oxide layer and the middle section of the drift region and is associated with a second RESURF structure. The doped region is isolated from the collector/emitter region and the emitter/collector region. A substrate contact (154) is disposed below the substrate and is coupled to the substrate. The doped region is isolated from the collector/emitter region by the drift region.

USE - For use in a variety of power, control and electronic applications, such as in motor controllers, in motor drives and in

appliance control. Also for use in a matrix switch or a voltage source converter.

ADVANTAGE - Has increased voltage blocking capability. Can block over 1200 volts in both directions.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of the bidirectional IGBT.

IGBT (100)
Emitter/collector contact (102)
Collector/emitter contact (104)
Substrate (150)
Substrate contact (154)
Drift region (160)
Oxide layer (170)
P-type region (177)
pp; 18 DwgNo 4/7

48/3,AB/6 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012704800
WPI Acc No: 1999-510909/199943
XRAM Acc No: C99-149463
XRPX Acc No: N99-380952
Fabricating capacitor over bit line structure for DRAM cell
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: BYUNG J P; PARK B; PARK B J
Number of Countries: 008 Number of Patents: 010
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2336031	A	19991006	GB 9826095	A	19981127	199943	B
FR 2776835	A1	19991001	FR 992960	A	19990310	199948	
DE 19860884	A1	19991014	DE 1060884	A	19981231	199949	
JP 11312792	A	19991109	JP 9987117	A	19990329	200004	
CN 1230778	A	19991006	CN 99100795	A	19990226	200006	
GB 2336031	B	20000517	GB 9826095	A	19981127	200026	
KR 99076229	A	19991015	KR 9810990	A	19980330	200051	
TW 390027	A	20000511	TW 98119254	A	19981120	200058	
US 6159820	A	20001212	US 99281023	A	19990330	200067	
KR 292940	B	20010712	KR 9810990	A	19980330	200226	

Priority Applications (No Type Date): KR 9810990 A 19980330
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2336031	A		24	H01L-021/8242	
FR 2776835	A1			H01L-021/8242	
DE 19860884	A1			H01L-021/8242	
JP 11312792	A		7	H01L-027/108	
CN 1230778	A			H01L-021/82	
GB 2336031	B			H01L-021/8242	
KR 99076229	A			H01L-027/108	
TW 390027	A			H01L-027/108	
US 6159820	A			H01L-021/20	
KR 292940	B			H01L-027/108	Previous Publ. patent KR 99076229

Abstract (Basic): GB 2336031 A
Abstract (Basic):

NOVELTY - The method involves forming a reverse photoresist pattern over a polysilicon layer, and etching the polysilicon layer, a second insulating layer, and a silicon nitride layer using the photoresist

pattern as a mask to form first openings. Sidewall spacers are formed, and second contact **holes** formed through to a contact pad.

DETAILED DESCRIPTION - Fabricating a capacitor over bit line (COB) structure for a DRAM cell, comprises:

(a) forming a first insulator layer (108) having bit line structures in it, over a **semiconductor** substrate (100) having **gate electrode** structures (104a-d) and contact pads (106a,b) between them;

(b) sequentially forming a silicon nitride layer (110) , a second insulating layer (112), and a polysilicon layer (114) over the first insulating layer;

(c) forming a reverse photoresist pattern (116) over the polysilicon layer;

(d) sequentially etching the polysilicon layer, the second insulating layer, and the silicon nitride layer using the photoresist pattern as a mask to form first openings (117);

(e) removing the photoresist pattern;

(f) forming sidewalls spacers (118), having etch selectivity with respect to the first insulating layer, from a first **conductive** layer on **lateral edges** of the first openings;

(g) etching the first insulating layer between the conductive sidewalls spacers to form self aligned second openings (119) to the contact pad;

(h) filling up the first and second openings with a second conductive layer;

(i) planarizing until the top surface of the second insulating layer is exposed; and

(j) etching the exposed second insulating layer using the silicon nitride layer as an etch stopper to form storage nodes (122) to the contact pads.

USE - For forming a DRAM capacitor.

ADVANTAGE - The storage node contact **holes** are formed in a self-aligned manner to the storage node, so the small contact **holes** are easily formed without misalignment to the bit line.

DESCRIPTION OF DRAWING(S) - The drawings shows cross-sections of the DRAM capacitor along the bit line direction during the manufacturing process.

Substrate (100)
Gate electrodes (104a-d)
Contact pads (106a,b)
First insulating layer (108)
Silicon nitride layer (110)
Second insulating layer (112)
Polysilicon layer (114)
Photoresist pattern (116)
First openings (117)
Sidewall spacers (118)
Second openings (119)
Storage nodes (122)
pp; 24 DwgNo 1B, 1G/2

48/3,AB/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012383561
WPI Acc No: 1999-189668/199916
XRAM Acc No: C99-055705
XRPX Acc No: N99-138758

Insulated gate field effect transistor with metal spacers
Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: DAWSON R; FULFORD H J; GARDNER M I; HAUSE F N; MICHAEL M W; MOORE B T; WRISTERS D J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5877058	A	19990302	US 96703272	A	19960826	199916	B

Priority Applications (No Type Date): US 96703272 A 19960826
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5877058	A		11	H01L-021/336	

Abstract (Basic): US 5877058 A
Abstract (Basic):
NOVELTY - The method comprises forming a non-floating **gate electrode** on a **gate** insulator formed on a **semiconductor** substrate, and forming sidewall insulators adjacent to the opposing **edges** of the **gate electrode**. A conductive metal layer is deposited over the substrate and an anisotropic etch applied to form metal spacers on the substrate and adjacent to the sidewall insulators, wherein the metal spacers contact first portions of the drain and the source and are electrically isolated from the **gate electrode**, and second portions of the drain and source outside the metal spacers are exposed.
USE - A method of forming an insulated gate field effect transistor with metal spacers.
ADVANTAGE - The metal spacers can be used as drain and source contacts, and increase **lateral conductivity** of lightly doped regions, thereby significantly reducing the resistance between heavily doped regions and the **channel**.
DESCRIPTION OF DRAWING(S) - The drawings show the formation of the IGFET
Semiconductor substrate (102)
Gate oxide (104)
Polysilicon layer (106)
Source and drain regions (120, 122)
pp; 11 DwgNo 1D,1F,2E/3

48/3,AB/8 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012039355
WPI Acc No: 1998-456265/199839
XRPX Acc No: N98-356018
Bidirectional lateral insulated gate bipolar transistor for bidirectional power switch - has RESURF structure positioned above substrate and below drift region and second RESURF structure positioned above drift region
Patent Assignee: ALLEN BRADLEY CO LLC (ALLB)
Inventor: LI H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5793064	A	19980811	US 96718842	A	19960924	199839	B

Priority Applications (No Type Date): US 96718842 A 19960924
Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
US 5793064 A 14 H01L-029/78

Abstract (Basic): US 5793064 A

The bidirectional lateral insulated gate bipolar transistor (100) , includes a **semiconductor** substrate (150). A drift region (160) is positioned above the substrate. A buried oxide layer (170) is positioned between the substrate and the drift region as a RESURF structure. An emitter/collector region is positioned above the first end of the drift region. The first portion of the emitter/collector region is more heavily doped with a first type dopant than the second portion. A collector/emitter region is positioned above the second end of the drift region. The first portion of the collector/emitter region is more heavily doped with the first type dopant than the second portion. A first region which is doped with a second type dopant is positioned above the emitter/collector region.

The second type dopant has an opposite conductivity type to the first dopant. A second region positioned above the collector/emitter region. The second region is doped with the second type dopant. A gate oxide layer is positioned above the middle section of the drift region. An emitter/collector contact (104) is coupled to the first region and the emitter/collector region. A collector/emitter contact (102) is coupled to the second region and the collector/emitter region. The drift region includes a **channel** area which **laterally conducts** current between the collector/emitter contact and the emitter/collector contact. Two **gate electrodes** (105,107) are coupled to the gate oxide layer and positioned above respective regions. A more heavily doped region than the drift region is positioned between the gate oxide layer and the middle section at the drift region. The doped region is associated with a second RESURF structure.

USE - For e.g. power, control and electronic application e.g. motor controllers, motor drives and appliance control.

ADVANTAGE - Conducts and blocks high voltages in both directions.

Dwg.6/8

48/3,AB/9 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010826044
WPI Acc No: 1996-322994/199633
Related WPI Acc No: 1999-108697
XRPX Acc No: N96-271770

Semiconductor transistor **edge** termination for **trenched** power MOSFET - has **channel** stop **trench** formed in substrate and conductive **channel** stop structure filling **trench** and extending over substrate principal surface adjacent **trench**

Patent Assignee: SILICONIX INC (SILI-N)
Inventor: HSHIEH F; YILMAZ H
Number of Countries: 006 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 722189	A2	19960717	EP 95120355	A	19951221	199633	B
JP 8264787	A	19961011	JP 9618399	A	19960109	199651	
US 5597765	A	19970128	US 95371174	A	19950110	199710	
			US 95423588	A	19950417		
EP 722189	A3	19970205	EP 95120355	A	19951221	199715	
US 5614751	A	19970325	US 95371174	A	19950110	199718	

			US 96632052	A	19960415	
KR 187763	B1	19990601	KR 96332	A	19960110	200055
EP 722189	B1	20010425	EP 95120355	A	19951221	200124
			EP 98111605	A	19951221	
DE 69520782	E	20010531	DE 620782	A	19951221	200138
			EP 95120355	A	19951221	

Priority Applications (No Type Date): US 95371174 A 19950110; US 95423588 A 19950417; US 96632052 A 19960415

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 722189	A2	E	14	H01L-029/06	
Designated States (Regional): DE FR IT					
JP 8264787	A		9	H01L-029/78	
US 5597765	A		12	H01L-021/44	Div ex application US 95371174
EP 722189	A3			H01L-029/06	
US 5614751	A		13	H01L-029/76	Cont of application US 95371174
KR 187763	B1			H01L-027/088	
EP 722189	B1	E		H01L-029/78	Related to application EP 98111605 Related to patent EP 895290
Designated States (Regional): DE FR IT					
DE 69520782	E			H01L-029/78	Based on patent EP 722189

Abstract (Basic): EP 722189 A

The transistor termination includes at least one active transistor body region formed in a substrate of one conductivity type and doped with a second conductivity type. A **trench** is formed in the active transistor body region, a **gate electrode** being formed in the **trench**.

A **channel** stop terminator is located at a perimeter of the transistor. A portion of the substrate of the first conductivity type is immediately adjacent to the terminator. The terminator includes a **channel** stop **trench** formed in the substrate and a conductive **channel** stop which fills the **trench** and extends over the substrate principal surface adjacent the **channel** stop **trench**.

ADVANTAGE - Prevents surface channelling without additional masking steps.

Dwg.2/6

Abstract (Equivalent): US 5614751 A

A **semiconductor** transistor device formed in a substrate of a first conductivity type and having a principal surface and comprising:

at least one active transistor body region formed in the substrate and doped a second conductivity type;

at least one **trench** formed in the substrate in the active transistor body region, a **gate electrode** being formed in the **trench**; and

a **channel** stop termination structure located in the substrate at a perimeter of the transistor and a portion of the substrate of the first **conductivity** type being immediately **laterally** adjacent the **channel** stop termination structure, the **channel** stop termination structure including:

a **channel** stop **trench** formed in the substrate; and

a conductive **channel** stop material filling the **trench** and extending over the principal surface adjacent the **channel** stop **trench**.

Dwg.2/6

US 5597765 A

A method of forming a **trenched semiconductor** transistor device including a **channel** stop, comprising the steps of:

providing a substrate having a principal surface and being doped with a dopant of a first conductivity type;

forming a field oxide layer on portions of the principal surface, the field oxide layer not being present on a portion of the principal surface towards an **edge** of the substrate which is a termination region of the transistor;

implanting a dopant of the first conductivity type into the entire principal surface, thereby forming a doped **channel** stop region in the termination region;

implanting a dopant of a second opposite conductivity type in a central portion of the substrate, thereby forming a body region of the transistor;

forming a **trench** in the central portion of the substrate; and

forming a conductive **gate electrode** in the **trench**

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Dwg.2/6f

48/3,AB/10 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010618761
WPI Acc No: 1996-115714/199612
Related WPI Acc No: 1995-214675
XRPX Acc No: N96-096778

Static random access memory - has **trench** extending through buried oxide layer, doped region and **semiconductor** layer adjacent **channel** region with conductive part partially within **trench** and adjacent gate dielectric layer acting as shared-**gate electrode**

Patent Assignee: MOTOROLA INC (MOTI)
Inventor: LAGE C S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5489790	A	19960206	US 94232968	A	19940425	199612	B
			US 95380772	A	19950130		

Priority Applications (No Type Date): US 94232968 A 19940425; US 95380772 A 19950130
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5489790	A		13	H01L-029/76	Div ex application US 94232968
					Div ex patent US 5422296

Abstract (Basic): US 5489790 A

The memory comprises a buried oxide layer overlying a P-type substrate (10) with an N-type doped region (21) overlying the buried oxide layer (13). A P-type **semiconductor** (22) layer overlies the doped region and a **trench** extends through the buried oxide layer, the doped region and **semiconductor** layer. The **trench** has a wall surface, a bottom surface, and a central region. A **channel** region of a transistor lies within the P-type **semiconductor** layer adjacent to the wall surface of the **trench**. A N-type doped region lies within the P-type **semiconductor** layer and adjacent to the wall surface. An N-type **semiconductor** layer overlies the substrate within the central region of the **trench** and has a wall surface which faces the wall surface of the **trench**.

A **channel** region of a second transistor lies within the N-type **semiconductor** layer and adjacent to the wall surface. Another P-type region lies within the N-type **semiconductor** layer. A gate dielectric layer lies adjacent to the wall surfaces of the **trench** and N-type **semiconductor** layer and adjacent to the bottom of the **trench** outside of the central region. A conductive part lies at least partially within the **trench** and adjacent to the gate dielectric layer. The **conductive** part **laterally** surrounds the N-type **semiconductor** layer and acts as a shared-**gate electrode** for the two transistors.

ADVANTAGE - Decrease chances of latch-up.

Dwg.14/15

48/3,AB/11 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010572043
WPI Acc No: 1996-068996/199607
XRPX Acc No: N96-057955

Charge coupled device with buried **channel** - has charge transport **channel** laterally bounded by region of opposite conductivity, **gate electrode** with two sub-regions either side of source zone extending between source zone and bounding region without overlap

Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG); PHILIPS ELECTRONICS NV (PHIG); PHILIPS NORDEN AB (PHIG); US PHILIPS CORP (PHIG)

Inventor: ROKS E

Number of Countries: 018 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9600452	A2	19960104	WO 95IB468	A	19950612	199607	B
WO 9600452	A3	19960215	WO 95IB468	A	19950612	199622	
EP 719456	A1	19960703	EP 95919604	A	19950612	199631	
			WO 95IB468	A	19950612		
JP 9502572	W	19970311	WO 95IB468	A	19950612	199720	
			JP 96502971	A	19950612		
US 5652442	A	19970729	US 95493045	A	19950621	199736	
EP 719456	B1	19990929	EP 95919604	A	19950612	199945	
			WO 95IB468	A	19950612		
DE 69512505	E	19991104	DE 612505	A	19950612	199953	
			EP 95919604	A	19950612		
			WO 95IB468	A	19950612		

Priority Applications (No Type Date): EP 94201799 A 19940623

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9600452	A2	E	17	H01L-029/768	
Designated States (National): JP					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
EP 719456	A1	E	1	H01L-029/768	Based on patent WO 9600452
Designated States (Regional): DE FR GB IT NL					
JP 9502572	W		18	H01L-027/148	Based on patent WO 9600452
US 5652442	A		9	H01L-027/148	
EP 719456	B1	E		H01L-029/768	Based on patent WO 9600452
Designated States (Regional): DE FR GB IT NL					
DE 69512505	E			H01L-029/768	Based on patent EP 719456
					Based on patent WO 9600452

WO 9600452 A3 H01L-029/768

Abstract (Basic): WO 9600452 A

The device includes a source zone in the centre of a CCD **channel** formed simultaneously with a **channel** bounding zone. A **gate electrode** comprises two parts on either side of the source zone which seen at the surface, do not overlap source and drain zones.

Below the **gate electrode**, a zone is formed with the same conductivity type of higher doping than the CCD **channel**. This forms a charge storage zone for the charge package to be read out. Source and drain zones are connected to the MOST **channel** region by an extension.

USE/ADVANTAGE - For imaging devices. Has high speed, high signal-to-noise ratio and high sensitivity.

Dwg.2/7

Abstract (Equivalent): US 5652442 A

A charge coupled device of the buried **channel** type comprising a **semiconductor** body which at a surface is provided with a charge transport **channel** in the form of a surface region of a first **conductivity** type which is **laterally** bounded in the **semiconductor** body by a bounding region of an opposite, second conductivity type and which is provided with a charge detector in the form of an insulated-gate surface-**channel** field effect transistor, a surface zone of the second conductivity type being provided locally in the charge transport **channel** so as to form a source zone of the field effect transistor, portions of the bounding region of the second conductivity type on either side of the charge transport **channel** forming a drain zone of the field effect transistor adjacent the source zone, and portions of the charge transport **channel** between the source and drain zones forming a **channel** region of the field effect transistor, characterized in that the **gate electrode** comprises two sub-regions which, seen at the surface, are situated on either side of the source zone and which extend between the source zone and the bounding region without overlap, at least one zone of the same conductivity type but with a higher doping concentration than that of the charge transport **channel** being provided in the charge transport **channel**, said zone extending at least for the major part exclusively below the sub-regions of the **gate electrode**, and the source and drain zones being provided with extensions of the second conductivity type which, seen at the surface, extend between the source and drain zones and the sub-regions of the **gate electrode**.

Dwg.1/7

48/3,AB/12 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010307516
WPI Acc No: 1995-208774/199528
Related WPI Acc No: 1998-144897; 1998-347599
XRAM Acc No: C95-096632
XRPX Acc No: N95-163597

Gate controlled lateral bipolar junction transistor device - for an integrated circuit which resembles a merged field effect transistor and a lateral bipolar transistor

Patent Assignee: MALHI D S (MALH-I); NORTHERN TELECOM LTD (NELE)
Inventor: DEEN M J; ILOWSKI J; KOVACIC S J; KUNG W; MALHI D S; DEEN M;

MAHLI D S
Number of Countries: 005 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 657944	A2	19950614	EP 94308956	A	19941202	199528	B
CA 2135981	A	19950610	CA 2135981	A	19941116	199536	
JP 7202051	A	19950804	JP 94331862	A	19941209	199540	
EP 657944	A3	19950802	EP 94308956	A	19941202	199613	

Priority Applications (No Type Date): US 93163636 A 19931209
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 657944	A2	E	19	H01L-029/739	
Designated States (Regional): DE FR GB					
JP 7202051	A		15	H01L-021/8249	
CA 2135981	A			H01L-027/07	
EP 657944	A3			H01L-029/739	

Abstract (Basic): EP 657944 A

A gate controlled lateral bipolar junction transistor (GCLBJT) for an IC comprises a substrate comprising a layer of **semiconductor** material of a first conductivity type having a surface and an underlying heavily doped **semiconductor** layer of the first conductivity type, first and second laterally spaced apart regions of a second conductivity type defined in the surface of the **semiconductor** layer and forming an emitter and a collector of the transistor, part of the layer of **semiconductor** material of the first **conductivity** type extending **laterally** between the emitter and the collector and forming a base region of the transistor, and lightly doped regions of the second conductivity type being provided in parts of the surface between emitter and collector, adjacent and contiguous with the emitter and collector regions, a **gate electrode** formed on the surface of the substrate overlying the base region and isolated therefrom by a gate dielectric, the heavily doped buried layer of the first conductivity type extending under the emitter, base and collector regions and forming a buried base electrode with a heavily doped base contact extending from the surface to the buried layer, first, second and third terminals being provided to the emitter, base and collector, for operation of the device as a bipolar transistor, and a fourth terminal being provided to the **gate electrode** for controlling surface inversion of a surface MOSFET **channel** provided by the base region under the **gate electrode** between emitter and collector regions, thereby providing for concurrent control of both field effect and bipolar injection phenomena in the base region during operation of the transistor with a potential on the **gate electrode**, for controlling a current path of minority carriers through the base region.

A method of operating and a method for fabrication are claimed.

USE - Gate controlled lateral bipolar junction transistor for ICs, e.g. mixer and modulator circuits.

ADVANTAGE - Common-emitter current gain, unity-gain frequency and low frequency noise properties are programmable, reduced noise and variable current gain over a wide range, concurrent use of field effect and bipolar injection phenomena.

Dwg.2/12

48/3,AB/13 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009995671
WPI Acc No: 1994-263382/199432
XRAM Acc No: C94-120549
XRPX Acc No: N94-207237
Forming dual polarity source and drain extensions in lateral complementary **channel** MOS - by forming PMOS in N **semiconductor** layer and NMOS in second, and **gate** -insulator and -**electrodes**,giving extensions self-aligned to gate
Patent Assignee: HARRIS CORP (HARO)
Inventor: BEASOM J D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5338960	A	19940816	US 92925077	A	19920805	199432	B

Priority Applications (No Type Date): US 92925077 A 19920805
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5338960	A		11	H01L-029/68	

Abstract (Basic): US 5338960 A
A method of mfg. CMOS architecture comprises forming a PMOS (40) in an N-**semiconductor** layer and an NMOS (50) in a second, P, portion, both having spaced P- or N- sources and drains respectively (44,45,54,55) and gate insulator (46,56) and **gate electrodes** (47,57) above **channel** regions. Respective dual **conductivity lateral** extension regions (61,71,81,91) extend from and are contiguous with at least one of source and drain towards the PMOS **channel** region and the NMOS **channel** region respectively. Each extension contains a portion of first conductivity type overlying and contacting a portion of second conductivity type.
Also claimed are (a) a method as above in which the dual **conductivity lateral** extension regions are formed simultaneously and also comprise third and fourth extension regions of first and second type respectively; (b) a method as above in which the insulated gate structures are used as masks for P- and N- implants to different depths to form the dual **conductivity lateral** extensions, and (c) the CMOS architecture formed as above.
USE/ADVANTAGE - For CMOS devices needing different reverse breakdown characteristics are for analogue multiplexes and switching circuits. The number of additional process steps is reduced by using common implants for NMOS and PMOS; breakdown characteristics are improved.
Dwg.2/6

48/3,AB/14 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008615079
WPI Acc No: 1991-119109/199117
XRPX Acc No: N91-091717
Opposite conductivity type MOSFET(s) - surrounded by high impurity annular region extending to buried region, with drain of one connected to gate of other
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: SHIRAI K

Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 423826	A	19910424	EP 90120127	A	19901019	199117	B
JP 3133171	A	19910606	JP 89272074	A	19891019	199129	
US 5087954	A	19920211	US 90598206	A	19901016	199209	
KR 9305509	B1	19930622	KR 9016610	A	19901018	199425	
EP 423826	B1	19960717	EP 90120127	A	19901019	199633	
DE 69027831	E	19960822	DE 627831	A	19901019	199639	
			EP 90120127	A	19901019		

Priority Applications (No Type Date): JP 89272074 A 19891019
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 423826	B1	E	13	H01L-027/092	
Designated States (Regional): DE FR GB					
DE 69027831	E			H01L-027/092	Based on patent EP 423826
KR 9305509	B1			H01L-027/092	

Abstract (Basic): EP 423826 A

An integrated circuit includes an n=**channel** MOSFET and a level shifting p=**channel** MOSFET formed in the same island region of a **semiconductor** substrate (1). The island is bounded by a high impurity concentration buried region (3) to which a similar annular contact region (8) extends.

The sources and drains of both MOSFETS are formed in the epitaxial material (4) which forms the island, and a conductive layer (26) provides the contacts therefor. The drain (11) of the p=**channel** MOSFET is thereby connected to the gate (14) of the n=**channel** MOSFET.

ADVANTAGE - Increased speed of operation and reduced power consumption. (12pp Dwg.No.2/4

Abstract (Equivalent): EP 423826 B

A MOS-type integrated circuit comprising: a **semiconductor** substrate (1) of a first conductivity type; a **semiconductor** layer (4) of a second conductivity type, on the **semiconductor** substrate; a buried region (3) of the second conductivity type, having high impurity concentration and formed between the **semiconductor** substrate (1) and **semiconductor** layer (4); an annular contact region (8) of the second conductivity type, extending from the buried region (3) to the surface of the **semiconductor** layer (4), surrounding the **semiconductor** layer (4) and having high impurity concentration; a first region (17) of the second conductivity type formed in contact with the second conductivity-type annular contact region (8), having low impurity concentration and extending into the **semiconductor** layer (4); a third region (24) of the first conductivity type and a second region (21) of the second conductivity type, which have high impurity concentration and which are formed in contact with each other in the first region (17) of the second conductivity type; a first region (11) of the first conductivity type, formed in the **semiconductor** layer (4), having low impurity concentration and being in contact with the first region of the second conductivity type; a fourth region (23) of the first conductivity type having high impurity concentration and formed in the first region (11) of the first conductivity type; a second region (16) of the first conductivity type having low impurity concentration and formed in the upper surface of the **semiconductor** layer (4) of the second conductivity type surrounded by the annular contact region (8) and laterally spaced from the first region (17) of the second **conductivity** type and **laterally** spaced from the first

region (17) of the second **conductivity** type and **laterally** spaced from the first region (11) of the first conductivity type; a third region (19) of the second conductivity type, a fifth region (22) of the first conductivity type, and a fourth region (20) of the second conductivity type, which have high impurity concentration, and are formed in the second region (16) of the first conductivity type, whereby said fifth region (22) is located between and in contact with the third (19) and fourth (20) regions of the second conductivity type; an insulating layer (25) covering junctions which are formed by the regions of different conductivity types and formed on the **semiconductor** layer of the second conductivity type and the annular contact region; a first polycrystal silicon layer (15) buried in the insulating layer (25) at a location corresponding to the first region (17) of the second conductivity type, and between the first region (11) of the first conductivity type, and the third region (24) of the first conductivity type; a second polycrystal silicon layer (14) buried in the insulating layer (25) at a location corresponding to the second region (16) of the first conductivity type, and surrounding the third region (18) of the second conductivity type, the fifth region (22) of the first conductivity type, and the fourth region (20) of the second conductivity type; a drain electrode electrically connected to the third region (24) of the first conductivity type and to the second region (21) of the second conductivity type through the insulating layer, and projecting from the surface of the insulating layer (25); a source electrode electrically connected to the fifth region (22) of the first conductivity type, and to the third (19) and fourth (20) regions of the second conductivity type through the insulating layer and projecting from the surface of the insulating layer (25); first and second **gate electrodes** electrically connected to the first and second polycrystal layers through the insulating layer and projecting from the surface of the insulating layer (25).

(Dwg.1/4

Abstract (Equivalent): US 5087954 A

The MOS integrated circuit includes a **semiconductor** layer of a second conductivity type, formed on a **semiconductor** substrate. A buried region of the second conductivity type, has high impurity concentration formed bytween the substrate and layer. An annular contact region of the second conductivity type, extend from the buried region to the surface of the second conductivity-type **semiconductor** layer and has high impurity concentration.

A drain and a gate of a MOSFET of a first conductivity **channel** type, and a source and a gate of a MOSFET of a second conductivity **channel** type are formed in that region of the second conductivity-type **semiconductor** layer which is defined by the annular contact regions. The second conductivity-type **semiconductor** layer is used for sources and drains of the MOSFETs, and a drain electrode of the MOSFET o the first conductivity **channel** type is connected to a **gate electrode** of the MOSFET of the second conductivity **channel** type.

ADVANTAGE - Saves power consumption of output circuit having high breakdown voltage and increases the operation speed of the circuit.

(10pp

48/3,AB/15 (Item 14 from file: 350)

008563500
WPI Acc No: 1991-067535/199110

XRAM Acc No: C91-028545
XRPX Acc No: N91-052257
SOI-MOS transistor with **conducting lateral** wall - has mono crystalline P-type silicon island with drain and source and lateral wall covered by insulating layer and polysilicon
Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Inventor: NISHIMURA T; YAMANO T
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2649831	A	19910118	FR 908962	A	19900713	199110	B
JP 3129777	A	19910603	JP 90133001	A	19900523	199128	
US 5060035	A	19911022	US 90550583	A	19900710	199145	

Priority Applications (No Type Date): JP 90133001 A 19900523; JP 89180952 A 19890713

Abstract (Basic): FR 2649831 A
The transistor is obtd. on a p-type substrate (1) covered by a layer of silicon oxide (2). An island of monocrystalline p-type silicon (3) is formed on the silicon oxide. This island supports the source and the drain of the transistor. A **channel** (33) is defined between the drain and source, while the transistor gate (7) is defined by layers of oxide and polycrystalline silicon deposited on the **channel** region.
A thin insulating layer (4) is deposited on the lateral wall of the silicon island. This layer is subsequently covered by polycrystalline p+ doped silicon (5). A lateral wall (8) separates the layer from the gate. An insulating interlayer (9) is formed by CVD on the silicon island. Contact **holes** (11,12) are provided in this interlayer, while an interconnection aluminium layer passes through one of the **holes** (11).
USE/ADVANTAGE - For CMOS inverter. Has improved electrical characteristics and reduced current produced by parasitic MOS in lateral walls. Creates voltage barrier next to transistor drain. Prevents voltage variations in substrate region. (44pp Dwg.No.2A/17
Abstract (Equivalent): US 5060035 A
Semiconductor device comprises an island-shaped **semiconductor** layer formed on major surface of an insulating surface and being isolated from any surrounding structures, source and drain regions, **gate electrode** formed on the **channel** surface through an insulating film, a sidewall insulating film formed on a sidewall along the periphery, a **semiconductor** sidewall layer with potentials of the source region and **semiconductor** sidewall layer being held the same.
ADVANTAGE - Electrical characteristics of a transistor in a SOI-MOS transistor is stabilised. (17pp

48/3,AB/16 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008060633
WPI Acc No: 1989-325745/198945
XRPX Acc No: N89-248001
Switchable power **semiconductor** with insulated gate bipolar transistors - has unit cells associated with MOS controlled thyristors turned-off by field-effect-controlled short-circuit
Patent Assignee: ASEA BROWN BOVERI AG (ALLM); ASEA BROWN BOVERI A (ALLM

)
Inventor: BAUER F
Number of Countries: 012 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 340445	A	19891108	EP 89105333	A	19890325	198945	B
JP 2012969	A	19900117	JP 8999898	A	19890419	199009	
US 4967244	A	19901030	US 89334967	A	19890407	199046	
EP 340445	B1	19930825	EP 89105333	A	19890325	199334	
DE 58905355	G	19930930	DE 505355	A	19890325	199340	
			EP 89105333	A	19890325		

Priority Applications (No Type Date): CH 881520 A 19880422
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 340445	A	G	7		
Designated States (Regional): AT BE CH DE FR GB IT LI NL SE					
EP 340445	B1	G	8	H01L-029/74	
Designated States (Regional): AT BE CH DE FR GB IT LI NL SE					
DE 58905355	G			H01L-029/74	Based on patent EP 340445

Abstract (Basic): EP 340445 A

The MOS contro-led thyristor (MCT) responsible for the turn-off process is associated with an insulated gate bipolar transistor (IGBT) whose p-type emitter layer (9) and n-type base layer (8) are of continuous form. The heavily-doped p-type region (13) is bounded laterally by p-doped **channel** regions (12) and inlaid n+ doped source regions (11), which with the n-type base layer (12) form an n-**channel** MOSFET.

The IGBT unit cell guarantees the turn-off of the thyristor. **Gate electrodes** (3) are held pref. at the same potential so that adjacent MCT and IGBT unit cells are controlled by the same gate.

ADVANTAGE - Can be optimised easily with regard to **channel** length, and affords more flexibility in respect of layout of component.

3/3

Abstract (Equivalent): EP 340445 B

Power **semiconductor** component with turn-off facility in which (a) next to each other and connected in parallel in a **semiconductor** substrate (14) between an anode (A) and a cathode (K); (b) each of said first unit cells is constructed as an MOS-controlled thyristor (MCT = MOS Controlled Thyristor) which can be turned off by means of a field-effect-controlled short circuit; (c) each of the first unit cells comprises, between the anode and the cathode a layer sequence composed of a p+ -doped p-type emitter layer, an n-doped n-type base layer, a p-doped p-type base layer (7) and an n+-doped n-type emitter region (6) with laterally adjacent n-doped **channel** regions (5) and embedded p+-doped source regions (4); (d) in each of the first unit cells, the source regions, the **channel** regions and the p-type base layer emerge next to each other at the cathode-side surface of the **semiconductor** substrate and in each case form an n-**channel** MOSFET with an insulated **gate electrode** (3) situated above it; and (e) additional means are provided which ensure the field effect controlled turning-on of the component; characterised in that (f) the additional means comprise second unit cells which, independently of the first unit cells, are arranged between the latter and are connected in parallel with the latter; (g) each of the second unit cells has the structure of a bipolar transistor with insulated gate (IGBT = Insulated Gate Bipolar Transistor), in which (h) each of the second unit cells comprises, between the anode and the cathode, a layer sequence composed of a p+

-doped p-type emitter layer, an n-doped n-type base layer, and a p+ -doped p-type region (13), embedded in the n-type base layer, with laterally adjacent p-doped **channel** regions (12) and embedded n+-doped source regions (11); (i) in each of the second unit cells, the source regions, the **channel** regions (1) and the n-type base layer emerge next to each other at the cathode-side surface of the **semiconductor** substrate and in each case form an n-**channel** MOSFET with an insulated **gate electrode** situated above it; (k) the source regions and the p+-type region are connected directly to the cathode via a cathode contact; and (i) the p-type emitter layers and the n-type base layers of both unit cells are in each case part of a common p-type emitter layer (9) or n-type base layer (8) respectively extending laterally over the **semiconductor** substrate.

(Dwg.1/3

Abstract (Equivalent): US 4967244 A

The component consists of a number of unit cells arranged parallel to each other. Each cell is a MOS- controlled thyristor (MCT) which can be switched off by a field-effect-controlled short circuit. Bipolar-transistor-with-insulated-gate (IGBT) cells connected in parallel with the MCT unit cells ensure switching on.

Each MCT unit cell has a sequence of heavily doped emitter and medium doped base layers of different conducting types forming a first conductivity-type-**channel** MOSFET with an insulated **gate electrode** above it. The IGBT unit cells form a second conductivity type-**channel** MOSFET with an insulated **gate electrode** above it. The p-type emitter layers and the n-type base layers of both elementary cells are in each part of a commen p-type emitter layer or n-type base layer respectively extending **laterally** over the semi-**conducted** substrate.

ADVANTAGE - Improved switch-on capability and increased flexibility in designing component

48/3,AB/17 (Item 16 from file: 350)

007728003

WPI Acc No: 1988-361935/198851

XRPX Acc No: N88-274124

High-voltage MOS transistor with IGFET - has double-sided junction gate FET on same **chip** with field effect **gate** pinching-off extended drain region

Patent Assignee: POWER INTEGRATIONS (POWE-N); POWER INTEGRATIONS INC (POWE-N)

Inventor: EKLUND K H

Number of Countries: 003 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 295391	A	19881221	EP 88106404	A	19880421	198851	B
JP 63314869	A	19881222	JP 88100015	A	19880422	198906	
US 4811075	A	19890307	US 8741994	A	19870424	198912	
EP 295391	B	19910130				199105	
DE 3861707	G	19910307				199111	
JP 8172184	A	19960702	JP 88100015	A	19880422	199636	
			JP 95196950	A	19880422		

Priority Applications (No Type Date): US 8741994 A 19870424

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

EP 295391 A E 9
US 4811075 A 6
JP 8172184 A 7 H01L-029/78 Div ex application JP 88100015

Abstract (Basic): EP 295391 A

A p-**channel** high-voltage MOS transistor a p-type silicon substrate (11) with a pair of pockets (35,36) of p+ conductivity adjoining the substrate surface. A source contact (31) is connected to one pocket and a drain contact (32) is connected to the other pocket. An extended drain region (37) of p-type material extends laterally on either side from the drain contact pocket.

A top layer (39) of n-material is ion- through the same window of the mask as the extended drain region to cover an intermediate part of it. The top layer material and the substrate are subjected to a reverse-bias voltage. The polysilicon gate (34) on the insulating SO2 layer (12) forms a **channel** laterally between the source contact pocket and extended drain region, and controls by field-effect the flow of current under it through the **channel**.

ADVANTAGE - Highly efficient MOS transistor is provided which is compatible with five volt logic and has figure of merit Ron by A of two ohms mm square.

2/5

Abstract (Equivalent): EP 295391 B

A high voltage MOS transistor (10; 30) comprising: a **semiconductor** substrate (11) of a first conductivity type having a surface, a pair of laterally spaced pockets (21, 24) of **semiconductor** material of a second conductivity type within the substrate and adjoining the substrate surface, a source contact (14) connected to one pocket (21), a drain contact (16, 32) connected to the other pocket (24), a drain region (26) of the second **conductivity** type extending **laterally** from the drain contact pocket (24) to a surface-adjoining position, a surface-adjoining layer (27) of material of the first conductivity type on top of an intermediate portion of the drain region (26) between the drain contact pocket (24) and the surface-adjoining position, said substrate (11) being subject to application of a reverse-bias voltage, an insulating layer (12) on the surface of the substrate (11) and covering at least that portion between the source contact pocket (21) and the nearest surface-adjoining position of the drain region (26), and a **gate electrode** (17) on the insulating layer (12) and electrically isolated from the substrate region thereunder which forms a **channel** laterally between the source contact pocket (21) and the nearest surface-adjoining position of the drain region (26), said gate lelectrode (17) controlling by field-effect the flow of current thereunder through the **channel**, characterized in that said drain region (26) is an extended one extending laterally each way from the drain contact pocket to the surface-adjoining positions, and said surface-adjoining layer (27) extends between the drain contact pocket (24) and the surface-adjoining positions and is physically connected to said substrate (11;33) so that biasing said substrate (11) means also biasing said surface-adjoining layer (27). (9pp)

Abstract (Equivalent): US 4811075 A

The insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same chip to form a high-voltage MOS transistor.

An extended drain region is formed on top of a substrate of opposite conductivity-type material.

A top layer of material having a conductivity-type opposite that of he extended drain and similar to that of the substrate is provided by ion-implantation through the same mask window as the extended drain

region.

This top layer covers only an intermediate portion of the extended drain whic has ends contacting a silicon dioxide layer.

The top layer is either connected to the substrate or left floating. Current flow through the extended drain region can be controlled by the substrate and the top layer, which act as gates providing field-effects for pinching off the extended drain region therebetween A complementary pair of such high-voltage MOS transistors having opposite conductivity-type are provided on the same chip.

ADVANTAGE - Increased efficiency.

(6pp Dwg.No. 1/5)

48/3,AB/18 (Item 17 from file: 350)

DIALOG(R)File 350:Derwent WPIX

004417290

WPI Acc No: 1985-244168/198540

XRPX Acc No: N85-182755

Travelling wave field effect transistor - has source and drain protrusions connected by channels in underlying III-V **semiconductor** substrate, **channel** conductivity controlled by gate

Patent Assignee: PLESSEY OVERSEAS LTD (PLES)

Inventor: HOLDEN A J; OXLEY C H

Number of Countries: 008 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 156585	A	19851002	EP 85301713	A	19850313	198540	B
GB 2156152	A	19851002	GB 856557	A	19850313	198540	
JP 60213066	A	19851025				198549	
US 4675712	A	19870623	US 85714506	A	19850321	198727	
GB 2156152	B	19870715				198728	

Priority Applications (No Type Date): GB 847275 A 19840321

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 156585	A	E	13		

Designated States (Regional): DE FR IT NL SE

Abstract (Basic): EP 156585 A

A number of **lateral conductive** channels (22) underlie and are spaced apart along the length of the continuous **gate electrode** (50). The channels extend between the source and drain electrodes (30,40), thus defining a number of distributed active sites (52,54,56). Inductive coupling between the drain and **gate electrodes** provides feedback to sustain and enhance wave propagation.

The drain electrode (40) is of a meander configuration and balances the waves on the drain and gate transmission lines (40,50). The **gate electrode** is of a T-section shape at each of the active sites. A supportive substrate (10) used is of III-V **semiconductor** material.

ADVANTAGE - Exhibits enhanced gain for given gate width. Has simple structure.

1/5

Abstract (Equivalent): GB 2156152 B

A travelling-wave field-effect transistor comprising:- a supportive substrate of **semiconductor** material; a continuous elongate source **electrode**; a continuous elongate **gate electrode**; and,

a continuous elongate drain electrode; and including a plurality of **lateral conductive** channels underlying and spaced apart along the length of the **gate electrode** and extending between the source and drain electrodes, defining thus a plurality of distributed active sites; and inductive coupling between the drain and **gate electrodes**, to provide feedback to sustain and enhance wave propagation.

Abstract (Equivalent): US 4675712 A

A travelling-wave field-effect transistor has a support substrate of **semiconductor** material and continuous elongate electrodes - a source **electrode** a drain **electrode** and a **gate electrode**. Gain improvement is achieved by dividing the structure into active and passive sites and by providing inductive coupling to supply power feedback to the **gate electrode** and thereby to sustain and enhance guided wave propagation. At each active site, protrusions extend from the source electrode, and protrusions extend from the drain electrode. The parasitic capacitance at each passive site is thus minimized.

The source and drain protrusions are connected by channels in the underlying **semiconductor** substrate and the conductivity of these channels controlled by **gate** operation. The drain **electrode** has a meander configuration. The **gate electrode** is of T-section shape at each active site. (5pp)t

48/3,AB/19 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003468343
WPI Acc No: 1982-16287E/198209
High current MOSFET with low forward resistance - has high **conductivity channel** with uniform **lateral** doping under gate oxide
Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: HERMAN T; LIDOW A
Number of Countries: 009 Number of Patents: 014
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2082385	A	19820303	GB 8124588	A	19810812	198209	B
DE 3131727	A	19820311	DE 3131727	A	19810811	198211	
FR 2488733	A	19820219				198212	
SE 8104485	A	19820322				198214	
JP 57109376	A	19820707				198233	
CA 1165900	A	19840417				198420	
GB 2082385	B	19850206				198506	
US 4593302	A	19860603	US 80178689	A	19800818	198625	
CH 656745	A	19860715				198634	
US 4680853	A	19870721	US 86869109	A	19860530	198731	
DE 3131727	C	19871112				198745	
IT 1139374	B	19860924				198823	
SE 457035	B	19881121				198849	
US 4593302	B1	19980203	US 80178689	A	19800818	199812	

Priority Applications (No Type Date): US 80178689 A 19800818
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2082385	A		22		
US 4593302	B1		2	H01L-029/76	

Abstract (Basic): GB 2082385 A

A high current MOSFET having low forward resistance comprises (a) a **semiconductor** chip having parallel surfaces; (b) a lightly doped first-type portion extending from a first surface through (part of) the chip thickness; (c) local second-type regions (220,221) in the first surface, spaced from each other by a symmetric mesh of body portions; (d) first type source regions (170,171) in and of lesser depth than the local regions, with the outer periphery of each a fixed distance from the periphery of the local region to define short conduction channels capable of inversion; (e) a mesh-shaped gate insulator (131) over the mesh between local regions and overlapping the short channels; (f) a mesh-shaped **gate electrode** (132) on the **gate** insulator; and (g) a vertical conductive first-type region (130) of higher dopant concentration than the body, extending from under the gate insulator between adjacent local regions to a depth less than the local regions, and having constant dopant concentration laterally across the first surface below the insulating layer.

Constant lateral doping concentration provides reduced parasitic base resistance without variation of gate width, increasing avalanche energy and reducing second breakdown problems, for high power switching.

22

48/3,AB/20 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

02525949
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 63-142849 [JP 63142849 A]
PUBLISHED: June 15, 1988 (19880615)
INVENTOR(s): SENDA KOJI
FUJII EIJI
HIROSHIMA YOSHIMITSU
APPLICANT(s): MATSUSHITA ELECTRONICS CORP [000584] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-291078 [JP 86291078]
FILED: December 05, 1986 (19861205)
JOURNAL: Section: E, Section Number 673, Volume 12, Number 402, Pg. 156, October 25, 1988 (19881025)

ABSTRACT

PURPOSE: To obtain C-MOS having SOI structure having no latch-up by forming PMOS onto an Si substrate, shaping a recrystallized silicon film onto an SiO(sub 2) film formed in regions except the transistor region of PMOS and shaping NMOS to the recrystallized silicon film.

CONSTITUTION: An n(sup +) **channel** stop region is formed to the transistor region 10 of a PMOS.Tr 4 and the peripheral of the region 10 by an SiO(sub 2) film 2 through an LOCUS process to an n-type Si substrate 1. When polysilicon 11 is irradiated with beams such as laser beams and electron beams and **lateral** seeding is **conducted** in the substrate, polysilicon 12 on the SiO(sub 2) film 2 is changed into excellent recrystallized silicon. Boron is implanted so that a recrystallized silicon film is brought to a p-type. The recrystallized silicon film 12 except the transistor region of an NMOS.Tr 3 is removed through a dry etching process. A **gate electrode** 13 is shaped through a conventional CMOS process, and source-drain in the PMOS.Tr4 and the NMOS.Tr3 are formed, thus manufacturing a CMOS.

48/3,AB/21 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

02246476
MANUFACTURE OF **SEMICONDUCTOR** MEMORY DEVICE

PUB. NO.: 62-163376 [JP 62163376 A]
PUBLISHED: July 20, 1987 (19870720)
INVENTOR(s): SUGAYA SHINJI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-005310 [JP 865310]
FILED: January 14, 1986 (19860114)
JOURNAL: Section: E, Section Number 570, Volume 12, Number 3, Pg. 42, January 07, 1988 (19880107)

ABSTRACT

PURPOSE: To reduce the width of an element isolation region so as to make EPROM highly integrated, by putting the element isolation region in self-alignment to a floating **gate electrode** so that it be formed to be equal to the gap of the floating **gate electrode** in the direction of a gate width.

CONSTITUTION: A first gate insulation film 3 is formed on a one conductivity type **semiconductor** substrate 1, and a first conductor layer PA is formed there on. Next, an isolation **groove** 11 whose base portion reaches the inside of the substrate 1 and which extends toward the direction of the gate length of a cell transistor to be formed on the surface of the substrate is formed, and the inside of the **groove** 11 is filled up with an insulation film 12. then, a second gate insulation film 6 is formed on the exposed surface of a divided conductor layer PA pattern, and a second conductor layer PB is formed. Subsequently, with the patterns of the conductor layers PB and PA aligned to a one mask pattern, patterning is made in th shape of a strip in the direction intersecting the isolation **groove** 11, so as to form a control **gate electrode** 7 made up of the conductor layer PB and a floating **gate electrode** 5 provided below the electrode 7 and made up of the **conductor** layer PA whose **lateral** side is self- aligned to the lateral side of the control **gate electrode** 7.

48/3,AB/22 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

01204152
SEMICONDUCTOR DEVICE

PUB. NO.: 58-141552 [JP 58141552 A]
PUBLISHED: August 22, 1983 (19830822)
INVENTOR(s): YAMAZAKI SHUNPEI
APPLICANT(s): SEMICONDUCTOR ENERGY LAB CO LTD [470730] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-024994 [JP 8224994]
FILED: February 18, 1982 (19820218)
JOURNAL: Section: E, Section Number 210, Volume 07, Number 255, Pg. 127, November 12, 1983 (19831112)

ABSTRACT

PURPOSE: To unify a phototransistor array onto the same substrate also including a peripheral circuit, and to form the array at low cost through a low process which does not exist in a single crystalline **semiconductor** by laminating NIPIN or PINIP type **semiconductors** onto the substrate and forming an IGFET with a **channel** forming region into IPI or INI regions.

CONSTITUTION: A metallic film 2 made of Ni, Cr, Mo(sub 1)Si, etc. is buried into the insulating substrate such as a glass or alumina substrate, and the surface is formed as approximately the same plane as the substrate. A metallic or **semiconductor** layer constituting a **gate electrode** is laminated again. The film is etched, and the **gate electrode** 12 is laminated and formed onto a gate insulator 11 in the **lateral** direction. A first **conductive** layer 2 shields incident light from the substrate side, and the IGFET20 is used as an IGFET having no photosensitivity merely. X-axis wiring is formed by first conductive layers 2, 3 and Y-axis wiring by a second conductive layer 9 in bipolar phototransistors 21, 22, and the phototransistors are constituted in matrix shape.

55/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6975353 INSPEC Abstract Number: B2001-08-2560R-046
Title: Numerical analysis on the LDMOS with a double epi-layer and **trench** electrodes
Author(s): Park, I.-Y.; Choi, Y.-I.; Chung, S.-K.; Lim, H.-J.; Mo, S.-I.; Choi, J.-S.; Han, M.-K.
Author Affiliation: Dept. of Molecular Sci. & Technol., Ajou University, Suwon, South Korea
Journal: Microelectronics Journal Conference Title: Microelectron. J. (UK) vol.32, no.5-6 p.497-502
Publisher: Elsevier,
Publication Date: May-June 2001 Country of Publication: UK
CODEN: MICEB9 ISSN: 0026-2692
SICI: 0026-2692(200105/06)32:5/6L.497:NALW;1-D
Material Identity Number: M243-2001-004
U.S. Copyright Clearance Center Code: 0026-2692/2001/$20.00
Conference Title: 5th International Seminar on Power Semiconductors. ISPS'2000. Proceedings
Conference Date: 30 Aug.-1 Sept. 2000 Conference Location: Prague, Czech Republic
Language: English
Abstract: We proposed a new lateral double-**diffused** MOS (LDMOS) structure employing a double p-n epitaxial layer, which is formed on p substrates. **Trenched** gate and drain are also employed to obtain uniform and high drift current density. The breakdown voltage and the specific on-resistance of the proposed LDMOS are numerically calculated by using the MEDICI 2D device simulator. The n drift region and upper p/sup -/ region of the proposed LDMOS are fully depleted in off-states employing the **RESURF** technique. The simulation results show that the breakdown voltage is 142 V and specific on-resistance is 183 m Omega .mm/sup 2/ when the cell pitch of the LDMOS is 7.5 mu m. The proposed LDMOS shows better trade-off characteristics than the previous results.
Subfile: B

55/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5422680 INSPEC Abstract Number: B9612-1210-039
Title: The fabrication process and optimum design of **RESURF** EDMOSFETs for smart power IC applications
Author(s): Jeong, H.-H.; Kwon, O.-K.
Author Affiliation: Dept. of Electron. English, Hanyang University, South Korea
Journal: Journal of the Korean Institute of Telematics and Electronics vol.33A, no.7 p.176-84
Publisher: Korea Inst. Telematics & Electron,
Publication Date: July 1996 Country of Publication: South Korea
CODEN: CKNOEZ ISSN: 1016-135X
SICI: 1016-135X(199607)33A:7L.176:FPOD;1-8
Material Identity Number: N523-96022
Language: Korean
Abstract: To overcome the drawbacks of conventional LDMOSFETs, we propose **RESURF** EDMOSFETs (**reduced surface field** extended drain MOSFETs) which can be adapted to various circuit applications, be driven without charge pumping circuitry and whose threshold voltage can be

adjusted. The devices have a **diffused** drift region formed by a high temperature process before gate oxidation. After polysilicon **gate electrode** formation, a fraction of the drift region around the gate **edge** is opened for supplemental self-aligned ion implantation to obtain a self-aligned drift region. This leads to a shorter gate length and desirable drift region junction contour under the gate **edge** for minimum specific on-resistance. In addition, a metal field plate in place of the field oxide makes it possible to simplify the fabrication processes and maximize the breakdown voltage. Also, by biasing the metal field plate, we can reduce the specific on-resistance further. The devices are optimized using the TSUPREM-4 process simulator and the MEDICI device simulator. The optimized devices have a breakdown voltage and specific on-resistance of 101.5 V and 1.14 m Omega .cm/sup 2/ for n-**channel RESURF** EDMOSFETs, and 98 V and 2.75 m Omega .cm/sup 2/ for p-**channel RESURF** EDMOSFETs. To check the validity of the simulations, we fabricated n-**channel** EDMOSFETs and confirmed a measured breakdown voltage of 97 V and specific on-resistance of 1.28 m Omega .cm/sup 2/. These results are superior to those of any other reported power devices for smart power IC applications.

Subfile: B

55/3,AB/3 (Item 1 from file: 350)

DIALOG(R)File 350:Derwent WPIX

014613993

WPI Acc No: 2002-434697/200246

XRAM Acc No: C02-123363

XRPX Acc No: N02-342196

Silicon carbide **semiconductor** device as metal-insulator-**semiconductor** field-effect transistor, includes P-type **gate electrode** and N-type impurity region having impurity **concentration** which form buried **channel** region

Patent Assignee: JAPAN SCI & TECHNOLOGY CORP (NISC-N); NAT INST ADVANCED IND SCI & TECHNOLOGY (NAAD-N); DOKURITSU GYOSEI HOJIN SANGYO GIJUTSU SO (DOKU-N); KAGAKU GIJUTSU SHINKO JIGYODAN (KAGA-N)

Inventor: ADACHI K; ARAI K; FUKUDA K; HARADA S; KOSUGI R; SENZAKI J

Number of Countries: 029 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020047125	A1	20020425	US 2001987271	A	20011114	200246	B
EP 1205981	A2	20020515	EP 2001309581	A	20011113	200246	
JP 2002151680	A	20020524	JP 2000346455	A	20001114	200250	
KR 2002037447	A	20020521	KR 200170801	A	20011114	200274	

Priority Applications (No Type Date): JP 2000346455 A 20001114

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020047125	A1		14	H01L-031/312	
EP 1205981	A2	E		H01L-029/78	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

JP 2002151680	A		9	H01L-029/78	
KR 2002037447	A			H01L-029/786	

Abstract (Basic): US 20020047125 A1

Abstract (Basic):

NOVELTY - A silicon carbide **semiconductor** device includes a

P-type **gate electrode** (8) formed on a gate insulation layer, and an N-type impurity region having an impurity concentration which form a buried **channel** region (2) on a lower surface of the gate insulation layer.

DETAILED DESCRIPTION - A silicon carbide (SiC) **semiconductor** device comprises a **semiconductor** substrate (1) having a P-type SiC region, a gate insulation layer formed on the SiC region; a P-type **gate electrode** formed on the **gate** insulation layer; an N-type impurity region having an impurity concentration to form a buried **channel** region on a lower surface of the gate insulation layer; and source and drain regions having N-type impurity regions formed adjacent to the gate insulation layer and **gate electrode**.

USE - As metal-insulator-**semiconductor** field-effect transistor on silicon carbide substrate.

ADVANTAGE - The SiC **semiconductor** device has increased **channel** mobility. The **channel** mobility is improved when optimizing the ratio between the source/drain junction depth and junction **depth** of the buried **channel** region junction. The surface orientation of the SiC substrate is optimized so that the device does not assume a normally on state. The device has high hot-carrier endurance and punch-through endurance.

DESCRIPTION OF DRAWING(S) - The figure depicts the fabrication of a metal-insulator-**semiconductor** field-effect transistor having a P-type **gate electrode** and buried **channel** region.

Semiconductor substrate (1)
Buried **channel** region (2)
P-type **gate electrode** (8)
pp; 14 DwgNo 1d/9

55/3,AB/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011529209
WPI Acc No: 1997-505690/199747
Related WPI Acc No: 1997-282492
XRAM Acc No: C97-161058
XRPX Acc No: N97-421177
MOS transistor of **reduced surface-field** strength type - is capable of preventing breakdown of elements at **channel**-forming portions, even if its drain undergoes voltage such as reverse voltage
Patent Assignee: DENSO CORP (NPDE); NIPPONDENSO CO LTD (NPDE)
Inventor: BAN H; FUJIMOTO H; IIDA M; IMAI H; KITAMURA Y; KOHNO K; MAEDA H; MIZUNO S; NAKAYAMA Y; SAITOU M; SAKAKIBARA T
Number of Countries: 005 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 802567	A2	19971022	EP 97106103	A	19970414	199747 B
JP 10004180	A	19980106	JP 96211675	A	19960809	199811
US 6242787	B1	20010605	US 96748896	A	19961115	200133
US 20020017697	A1	20020214	US 96748896	A	19961115	200214
			US 97834386	A	19970416	
			US 2001945621	A	20010905	

Priority Applications (No Type Date): JP 96250299 A 19960920; JP 9692769 A 19960415; JP 96211675 A 19960809; JP 95297148 A 19951115; JP 968699 A 19960122
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

EP 802567 A2 E 52 H01L-027/02
Designated States (Regional): DE FR IT
JP 10004180 A 18 H01L-027/08
US 6242787 B1 H01L-029/76
US 20020017697 A1 H01L-023/58 CIP of application US 96748896
Cont of application US 97834386
CIP of patent US 6242787

Abstract (Basic): EP 802567 A
The **semiconductor** device comprises: (a) a **semiconductor** layer (1) of first conductivity type; (b) a first well (16) of second conductivity type on the **semiconductor** layer; (c) a second well (2) of first conductivity type in the first well to be shallower than the first well; (d) a source region (4), a **channel** region, and a drain region (5) in the second well; and (e) a **gate electrode** (7) on the **channel** region so that the second well serves as a drift region, such that, when a voltage for setting the MOS transistor in to a non-actuating condition is applied to the **gate electrode**, and a high voltage exceeding a given value is applied to the drain region, a current-carrying path is made to extend from the second well through the first well and the **semiconductor** layer.
USE - Used in the field of **semiconductor** device manufacturing, especially lateral **diffused** MOS transistors.
ADVANTAGE - The MOS transistor is of **reduced surface-field** strength type which is capable of preventing the breakdown of elements at **channel**-forming portions, even if its drain undergoes a voltage such as the reverse voltage. A LDMOS and an NPNTr can be formed on the same substrate. The occurrence of switching noise is suppresses when a load-driving **semiconductor** element is provided in an insulated and separated regions. A power MOS transistor is formed able to withstand a high surge current.
Dwg.1/52

55/3,AB/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011304587
WPI Acc No: 1997-282492/199726
Related WPI Acc No: 1997-505690
XRPX Acc No: N97-233872
Laterally **diffused** MOS transistor device having **reduced surface field** - has n-type **semiconductor** layer and p-type trough, trough serving as drift region
Patent Assignee: DENSO CORP (NPDE); NIPPONDENSO CO LTD (NPDE)
Inventor: BAN H; FUJIMOTO H; IIDA M; IMAI H; MAEDA H; NAKAYAMA Y; SAITOU M; KITAMURA Y; KOHNO K; MIZUNO S; SAKAKIBARA T
Number of Countries: 003 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 19647324	A1	19970522	DE 1047324	A	19961115	199726 B
JP 9139438	A	19970527	JP 95297148	A	19951115	199731
JP 9266310	A	19971007	JP 96250299	A	19960920	199750
US 6104076	A	20000815	US 96748896	A	19961115	200041
JP 3114592	B2	20001204	JP 95297148	A	19951115	200065
US 6242787	B1	20010605	US 96748896	A	19961115	200133
US 20020017697	A1	20020214	US 96748896	A	19961115	200214
			US 97834386	A	19970416	
			US 2001945621	A	20010905	

Priority Applications (No Type Date): JP 968699 A 19960122; JP 95297148 A 19951115; JP 96211675 A 19960809
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19647324	A1		21	H01L-029/78	
JP 9139438	A		8	H01L-021/8249	
JP 9266310	A		9	H01L-029/78	
US 6104076	A			H01L-029/76	
JP 3114592	B2		9	H01L-021/8249	Previous Publ. patent JP 9139438
US 6242787	B1			H01L-029/76	
US 20020017697	A1			H01L-023/58	CIP of application US 96748896 Cont of application US 97834386 CIP of patent US 6242787

Abstract (Basic): DE 19647324 A

The MOS transistor has a **reduced surface field** strength and includes an n-type **semiconductor** layer and a p-type trough formed in the layer. An n-type trough is formed in the initial trough and it contains a source region, a **channel** region, and a drain region.

On the **channel** region is formed a **gate electrode** such that the p-type trough serves as a drift region. On voltage application, the MOS transistor is in non-active state. On application to the drain of a HV exceeding a preset value, a current path is formed. This path extends from the p-type trough over the n-type trough and the **semiconductor** layer.

USE/ADVANTAGE - For component with load control transistor, e.g. LDMOSFET, with breakdown prevention of **channel** forming elements on HV application to drain.

Dwg.1/16

55/3,AB/6 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010895758
WPI Acc No: 1996-392709/199639
XRPX Acc No: N96-330953
Insulated gate bipolar transistor - has P-type collector **diffusion** region formed in N- drift region being spaced from P- **resurf diffusion** region and having N+ collector region formed within it to define second invertible **channel**
Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: KINZER D M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5548133	A	19960820	US 94308556	A	19940919	199639	B

Priority Applications (No Type Date): US 94308556 A 19940919
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5548133	A		7	H01L-029/74	

Abstract (Basic): US 5548133 A

The IGBT includes a thin **semiconductor** wafer with a P+ substrate extending to one wafer surface with a P- body formed atop it and extending to another wafer surface. At least one P-type base region

is **diffused** into the P- body and an N-type emitter **diffusion** region formed in this base region to define an invertible **channel** region. A **MOS-gate** structure is disposed atop this invertible **channel** region.

An N- drift region is **diffused** into the P- body surface and it extends from the base region into which a relatively thick P- **resurf diffusion** region is formed and contained. A P-type collector **diffusion** formed in the drift region at a location spaced from the **resurf diffusion** region has an N+ collector **diffusion** region is formed in it to define a second invertible **channel** region between the N+ collector **diffusion** and N- drift regions upon which a second **MOS-gate** is disposed. Emitter and collector contacts are connected to the base and the P-type and N+ collector **diffusion** regions. Avalanche breakdown occurs from the P-type collector **diffusion** region to prevent avalanche breakdown from the P-type base region.

ADVANTAGE - Has improved ruggedness. Short circuit protection and overtemperature protection circuits are also integrated into chip. P+/N region causes breakdown to occur beneath P+ region away from critical **MOS-gate** region.

Dwg.4/5

55/3,AB/7 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010046860
WPI Acc No: 1994-314571/199439
XRPX Acc No: N94-247015

Dielectric isolated **semiconductor** device especially JFET - is supported by **semiconductor** body with base, oxide layer, and lightly N doped mono-crystalline substrate

Patent Assignee: TELEFONAKTIEBOLAGET ERICSSON L M (TELF)
Inventor: LITWIN A
Number of Countries: 013 Number of Patents: 012
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
SE 9300211	A	19940726	SE 93211	A	19930125	199439	B
SE 500815	B	19940912	SE 93211	A	19930125	199439	
JP 6260506	A	19940916	JP 945895	A	19940124	199442	
EP 623949	A1	19941109	EP 94850005	A	19940112	199443	
US 5432377	A	19950711	US 94185146	A	19940124	199533	
CN 1092557	A	19940921	CN 94100576	A	19940125	199716	
US 5741723	A	19980421	US 94185146	A	19940124	199823	
			US 95444512	A	19950519		
SG 49599	A1	19980615	SG 96621	A	19940112	199836	
EP 623949	B1	19981028	EP 94850005	A	19940112	199847	
DE 69414169	E	19981203	DE 614169	A	19940112	199903	
			EP 94850005	A	19940112		
SG 54996	A1	19981221	SG 96764	A	19940112	199929	
KR 307304	B	20020620	KR 941283	A	19940125	200279	

Priority Applications (No Type Date): SE 93211 A 19930125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SE 9300211	A		25	H01L-021/22	
SE 500815	B			H01L-021/22	
JP 6260506	A		9	H01L-021/337	
EP 623949	A1	E	16	H01L-021/22	

Designated States (Regional): CH DE FR GB IT LI NL

US 5432377	A	14	H01L-027/04	
CN 1092557	A		H01L-029/36	
US 5741723	A	14	H01L-021/76	Div ex application US 94185146 Div ex patent US 5432377
SG 49599	A1		H01L-021/22	
EP 623949	B1 E		H01L-029/06	

Designated States (Regional): CH DE FR GB IT LI NL

DE 69414169	E	H01L-029/06	Based on patent EP 623949
SG 54996	A1	H01L-021/76	
KR 307304	B	H01L-029/68	Previous Publ. patent KR 94019000

Abstract (Basic): SE 9300211 A

The **semiconductor** device has areas with reduced electrical field strength, and includes a component area (4) in a **semiconductor** body with an upper surface. A dielectric insulating layer (5) limits the component area from the **semiconductor** body. A lowered area (G1) in the component area which extends downwards from the upper surface, with a PN junction to remainder of the component area (4). There are electrical connecting areas (G2,D2) in each of the lower area and the remaining part of the component area (4).

The areas with reduced electrical field strength are depleted of carriers through electrical voltage (VG,VS,VD) connected through the electrical connecting areas. The component area has two opposite sides defined against the **semiconductor** body through the dielectric insulating layer (2).

ADVANTAGE - Simple prodn.

Dwg.1/14

Abstract (Equivalent): US 5432377 A

The dielectrically isolated **semiconductor** device includes charge carrier depleted regions of reduced electrical field strength, and is supported by a **semiconductor** body including a substrate, an oxide layer and a weakly doped monocrystalline wafer. **Trenches** for a dielectrically isolating layer which surrounds a component region are etched in the wafer.

A FET in the component region has two doped **wafer**-line **gate** regions, which have been **diffused** in the component region with the aid of a first mask. Two heavily doped regions are **diffused** in the component region with the aid of a second mask, these regions forming the source region and the drain region of the transistor.

ADVANTAGE - Simple mfr., with simple choice of masks; component region weakly doped and easy to deplete of charge carriers. FET withstands high voltages without risk of current breakthrough; component region occupies only relatively small area on substrate.

Dwg.1/14

59/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7860621 INSPEC Abstract Number: B2004-03-2560P-036
Title: 200V multi **RESURF trench** MOSFET (MR-TMOS)
Author(s): Kurosaki, T.; Shishido, H.; Kitada, M.; Oshima, K.; Kunori, S.; Sugai, A.
Conference Title: ISPSD'03. 2003 IEEE 15th International Symposium on Power Semiconductor Devices and ICs Proceedings (Cat. No.03CH37456) p. 211-14
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2003 Country of Publication: USA xxiii+389 pp.
ISBN: 0 7803 7876 8 Material Identity Number: XX-2003-00455
U.S. Copyright Clearance Center Code: 0 7803 7876 8/2003/$17.00
Conference Title: IEEE International Symposium on Power Semiconductor Devices and Integrated Circuits
Conference Sponsor: Univ. Cambridge; UK Eng. & Phys. Sci. Res. Council (EPSRC)
Conference Date: 14-17 April 2003 Conference Location: Cambridge, UK
Language: English
Abstract: In this paper, we propose a new structure of **trench** MOSFETs, named Multi **RESURF Trench** MOSFETs (MR-TMOS). This structure has a deep p type pillar under the **trench gate electrode** . This p type pillars are formed by using the method of filling **trenches** with epitaxial silicon. Using this technique, we have developed a 200V class low on-resistance MOSFETs with RonA=4.8 m Omega cm/sup 2/ at V/sub G/=10V and Vdss=245V. This experimental result shows superior characteristics and a relatively good agreement with the simulation result, RonA=5.0 m Omega cm/sup 2/ at V/sub G/=10V and Vdss=252V.
Subfile: B

59/3,AB/2 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01663642 AAD9903707
DESIGN AND CHARACTERIZATION OF 6H-SIC DEVICES FOR HIGH-POWER AND HIGH-TEMPERATURE APPLICATIONS (SILICON CARBIDE, INSULATED GATE BIPOLAR TRANSISTORS)
Author: RAMUNGUL, NUDJARIN
Degree: PH.D.
Year: 1998
Corporate Source/Institution: RENSSELAER POLYTECHNIC INSTITUTE (0185)
Source: VOLUME 59/08-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 4347. 244 PAGES

Silicon Carbide (SiC) offers great promise in high-temperature and high-power **semiconductor** device applications. This research focuses on the development of 6H-SiC devices with special emphasis on the two most important aspects in **semiconductor** power electronics, SiC PN junctions and the **MOS-gated** power devices.

The performances of four different types of SiC junction rectifiers: p$\sp+$n epitaxial junctions, p$\sp+$n implanted junctions, n$\sp+$p epitaxial junctions, and n$\sp+$p implanted junctions, have been extensively studied and compared with existing theories as well as simulation results. Factors that limit the performance of practical SiC

junctions have been identified and theoretically verified, ensuring that the deficiencies in present SiC rectifiers are not material inherent but are exclusively due to material quality and processing problems. By optimizing the implantation dosage, improving the devices design, and carefully calibrating fabrication process to minimize the chance of defect creation, SiC junction rectifiers with forward characteristics close to theoretical predictions and reversible breakdown characteristics have been realized for the first time.

The analytical models for the breakdown voltages of 6H-SiC have been developed and an analytical approach extending from existing models for Si IGBTs has been applied to SiC IGBTs performance analysis and optimization. High voltage 6H-SiC UMOS IGBTs have been designed, fabricated by using a fully planarized process, and functional IGBTs have been experimentally demonstrated for the first time. The IGBT operation at temperature up to 300$\sp\circ$C, the highest operation temperature ever reported on any IGBT, has been measured. Comparing to a SiC UMOS FET with the same design and process, the IGBT has approximately 30$\times$ higher output current capability due to minority carrier injection. Both devices exhibit a remarkably low leakage current $\rm ({<}10\sp{-7}\ A/cm\sp2\ at\ 100V)$ at temperature below 200$\sp\circ$C.

Various termination designs (JTE, **RESURF**, and a new three-step **trench** termination) have been analytically studied, designed and compared. Particularly, the three-step **trench** termination has been optimized, and implemented for SiC UMOS devices, yielding a breakdown voltage of 1000V, close to the design target of $\sim$1200V.

59/3,AB/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015291523
WPI Acc No: 2003-352456/200333
XRPX Acc No: N03-281492
Dual-gate power MOSFET includes independently biased **gate electrode** overlying channels formed in base region surrounding positively doped region, and drift region with alternating columns
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: BOSE A; KHEMKA V K; PARTHASARATHY V; ZHU R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6528849	B1	20030304	US 2000652813	A	20000831	200333	B

Priority Applications (No Type Date): US 2000652813 A 20000831
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6528849	B1		7	H01L-029/78	

Abstract (Basic): US 6528849 B1
Abstract (Basic):

NOVELTY - A **gate electrode** (77) is formed on a **channel** (91) formed in the base region (81) surrounding P+ region (83) depending upon voltage applied to the **gate electrode** and the drain region (92). The **gate electrode** is electrically biased independent of another **gate electrode** (78) on a **channel** (71). A drift region (94) coupled between the channels has alternating columns which are doped with N- and P-type impurities.

USE - **Reduced surface field** (**RESURF**) power

dual-gate metal oxide **semiconductor** field effect transistor (DMOSFET) in integrated circuits.

ADVANTAGE - The dual-gate depletion mode metal oxide **semiconductor** field effect transistor in its off state acts as both a NMOS device and a PMOS device. Therefore, the DMOSFET has greater conductivity and lower resistance in its on state than a single-gate **RESURF** superjunction lateral DMOSFET having a drift region of the same overall size. Reduction in the breakdown voltage of the dual-gate DMOSFET is reduced with decrease in the cross-sectional width of the drift region.

DESCRIPTION OF DRAWING(S) - The figure shows an explanatory diagram of the dual-gate **RESURF** superjunction lateral MOSFET.

channels (71,91)
gate electrodes (77,78)
base region (81)
P+ region (83)
drain region (92)
drift region (94)
pp; 7 DwgNo 4/4

59/3,AB/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010112921
WPI Acc No: 1995-014174/199502
XRAM Acc No: C95-006411
XRPX Acc No: N95-011051

Mfr of a lateral self-aligned DMOS transistor - using an n-**RESURF** region over a p substrate, maintains symmetry between adjacent transistor strips to eliminate hot spots and breakdown

Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: KWON O; NG W T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5369045	A	19941129	US 9386773	A	19930701	199502	B

Priority Applications (No Type Date): US 9386773 A 19930701
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5369045	A		7	H01L-021/265	

Abstract (Basic): US 5369045 A

A method of forming a DMOS transistor comprises forming an insulating layer (24) on a doped **semiconductor** layer (14), patterning to expose source (16) and drain (18) windows, and forming a D-well (20) by doping within the source region. A sidewall region is formed around the source window, source and drain regions are formed within the windows, and a **gate electrode** (26) formed over part of the D well between source and insulating layer and over a **channel** between source and drain.

Also claimed is a method as above in which an n-Si layer is formed over a p-substrate, field oxide is formed and patterned, B is implanted to form the D-well, and a nitride layer is formed over the oxide and windows, followed by sidewall oxide. Processing is then as above.

USE - In high density power devices for intelligent power IC's.

ADVANTAGE - Self-aligned symmetry is maintained between adjacent transistor strips which eliminates local hotspots and breakdowns and

differences in specific on-resistance and breakdown voltage.
Dwg.1/8

59/3,AB/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009988811
WPI Acc No: 1994-256522/199432
XRAM Acc No: C94-117223
XRPX Acc No: N94-202152
High voltage transistor for **semiconductor** integrated circuit - including a silicon-on-insulator region in which a source and **channel** are formed and with a drain drift region formed partly in the silicon-on-insulator and bulk silicon@ regions
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: MALHI S
Number of Countries: 009 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 610599	A1	19940817	EP 93121108	A	19931230	199432 B
JP 7007153	A	19950110	JP 9421780	A	19940104	199511
TW 277149	A	19960601	TW 94103568	A	19940422	199641
US 5554546	A	19960910	US 93317	A	19930104	199642
			US 94342398	A	19941118	
			US 95513056	A	19951017	
US 5686755	A	19971111	US 93317	A	19930104	199751
			US 94342398	A	19941118	
			US 96771371	A	19961216	
KR 325559	B	20020727	KR 949	A	19940103	200309

Priority Applications (No Type Date): US 93317 A 19930104; US 94342398 A 19941118; US 95513056 A 19951017; US 96771371 A 19961216
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 610599	A1	E	7	H01L-029/784	
Designated States (Regional): DE FR GB IT NL					
JP 7007153	A		6	H01L-029/78	
TW 277149	A			H01L-021/331	
US 5554546	A		5	H01L-021/8234	Cont of application US 93317 Div ex application US 94342398
US 5686755	A		6	H01L-023/58	Cont of application US 93317 Cont of application US 94342398
KR 325559	B			H01L-029/772	Previous Publ. patent KR 94019013

Abstract (Basic): EP 610599 A
A transistor comprises: a SOI region; a source formed in the SOI region; a drain drift region partly formed in the SOI region and partly formed beyond the SOI region in a bulk Si; a drain region formed in the drain drift region on the bulk Si; a **channel** formed in the SOI region between the source region and the drain drift region; and a gate coupled to the SOI **channel**. A method of fabricating is disclosed.
USE/ADVANTAGE - High voltage high-side driver **RESURF** LDMOS devices for **semiconductor** ICs. Electrical isolation is provided between source and substrate, low on-resistance characteristics, simplified planar structure.
Dwg.6/7
Abstract (Equivalent): US 5686755 A
A **semiconductor** device comprising:a substrate having a bulk

substrate region and a SOI substrate region; and a high voltage transistor located partly within the bulk substrate region and partly within the SOI substrate region, where the high voltage transistor comprises:.a source region located within the SOI substrate region;a drift region located in the bulk substrate region; a drain region located within the drift region;a **channel** region located within the SOI substrate region extending from the source region to the drift region; and a **gate electrode** extending over the **channel** region.

Dwg.6/6

US 5554546 A

A method for fabricating a **semiconductor** device comprises:

providing a substrate having a first conductivity type;

forming a body insulating layer in the substrate beneath a face of the substrate and spaced from the face;

forming a first doped region of a second conductivity type, the first doped region extending from the face into the substrate to a depth equal to or greater than the insulating layer and surrounding the body insulating layer, thereby isolating a **channel** region of the substrate between the face, the body insulating layer and the first doped region;

forming a first contact providing conductive contact to the first doped region;

forming a second doped region in the **channel** region, the second doped region having the second conductivity type and the second doped region being spaced from the first doped region;

forming a second contact providing conductive contact to the second doped region;

forming a gate insulating layer on the face over the portion of the **channel** region between the first and second doped regions; and

forming a gate on the gate insulating layer.

(Dwg.6/6

59/3,AB/6 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

009611181

WPI Acc No: 1993-304729/199339

XRAM Acc No: C93-135604

XRPX Acc No: N93-234410

High voltage structure with oxide isolated source - with drift region in bulk silicon@ giving low on resistance

Patent Assignee: TEXAS INSTR INC (TEXI)

Inventor: MALHI S

Number of Countries: 008 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 562271	A1	19930929	EP 93102538	A	19930218	199339	B
US 5338965	A	19940816	US 92857875	A	19920326	199432	
			US 9353028	A	19930426		
JP 6260652	A	19940916	JP 9368136	A	19930326	199442	
EP 562271	B1	19980114	EP 93102538	A	19930218	199807	
DE 69316256	E	19980219	DE 616256	A	19930218	199813	
			EP 93102538	A	19930218		
KR 301918	B	20011022	KR 934649	A	19930325	200236	

Priority Applications (No Type Date): US 92857875 A 19920326; US 9353028 A 19930426

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 562271	A1	E	7	H01L-029/784	
Designated States (Regional): DE FR GB IT NL					
US 5338965	A		6	H01L-027/01	Div ex application US 92857875
JP 6260652	A		6	H01L-029/784	
EP 562271	B1	E	10	H01L-029/772	
Designated States (Regional): DE FR GB IT NL					
DE 69316256	E			H01L-029/772	Based on patent EP 562271
KR 301918	B			H01L-029/94	Previous Publ. patent KR 93020739

Abstract (Basic): EP 562271 A

(I) High voltage power transistor comprising (a) **semiconductor**-on-insulator (SOI) transistor; (b) bulk **semiconductor** drain drift region connected to it. (II) Also claimed is a high side driver configuration with a high voltage power transistor having its source isolated from the substrate comprising: (a) drain drift region formed in a **semiconductor** substrate having a drain contact and an interconnect contact with the drain contact connected to a power supply; (b) SOI MOS as claim (I). (III) Also claimed is a method of forming a high voltage power transistor. (IV) Also claimed is a method of configuring a high voltage power transistor in a high side driver configuration.

USE/ADVANTAGE - The source isolated high voltage power transistor has a low 'on' resistance allowing its use in applications requiring electrical isolation between source and substrate.

Dwg.1/2

Abstract (Equivalent): EP 562271 B

(I) High voltage power transistor comprising (a) **semiconductor**-on-insulator (SOI) transistor; (b) bulk **semiconductor** drain drift region connected to it. (II) Also claimed is a high side driver configuration with a high voltage power transistor having its source isolated from the substrate comprising: (a) drain drift region formed in a **semiconductor** substrate having a drain contact and an interconnect contact with the drain contact connected to a power supply; (b) SOI MOS as claim (I). (III) Also claimed is a method of forming a high voltage power transistor. (IV) Also claimed is a method of configuring a high voltage power transistor in a high side driver configuration.

USE/ADVANTAGE - The source isolated high voltage power transistor has a low 'on' resistance allowing its use in applications requiring electrical isolation between source and substrate.

Dwg.0/3

Abstract (Equivalent): US 5338965 A

A high voltage power transistor comprises (a) a lateral SOI transistor and (b) a bulk **semiconductor** drain drift region. The SOI transistor comprises (i) an insulating layer over a **semiconductor** substrate, (ii) a three-section **semiconductor** layer, each section forming respectively a source for both the SOI and the high voltage power transistor, a **channel** and a drain, (iii) a 2nd insulating layer over the **channel** section, and (iv) a patterned conductive layer over the 2nd insulating layer, forming a **gate electrode** for both the SOI and the high voltage power transistor.

USE/ADVANTAGE - Used in **RESURF** LDMOS circuits. Low 'on' resistance, with electrical isolation between source and substrate. Isolated source and **RESURF** drift region.

Dwg.1/5

59/3,AB/7 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004327381
WPI Acc No: 1985-154259/198526
XRPX Acc No: N85-116471
Combined bipolar field effect transistor **resurf** device - exhibits lower requirement for base drive current for ON-state resistance and lower internal power dissipation
Patent Assignee: PHILIPS GLOEILAMPENFAB NV (PHIG)
Inventor: SINGER B M; STUPP E H; YAYARAMAN B
Number of Countries: 006 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 146181	A	19850626	EP 84201803	A	19841205	198526	B
JP 60153163	A	19850812	JP 84266066	A	19841217	198538	
CA 1220875	A	19870421				198720	
EP 146181	B	19890315				198911	
DE 3477313	G	19890420				198917	

Priority Applications (No Type Date): US 83562145 A 19831216; US 83562144 A 19831216
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 146181	A	E	17		
Designated States (Regional): DE FR GB NL					
EP 146181	B	E			
Designated States (Regional): DE FR GB NL					

Abstract (Basic): EP 146181 A

A p-type **semiconductor** substrate (11) has a lightly-doped (3.10.14) epitaxial buried layer (16) on its major surface, which is about thrity microns thick and is p-conductivity type. An n-type epitaxial surface layer (18), of doping concentration and thickness chosen according to the **reduced surface field** technique, is disposed in the buried layer (16). A surface adjoining p-conductivity base region (20) has a base electrode (22) and forms part of a vertical pnp transistor. A surface-adjoining n+ conductivity combined source-emitter region (24) is formed with a source-emitter electrode (26).

An n+conductivity drain collector region (28) is adjacent to the surface layer (18) and spaced from the base connected to an electrode (30). A lateral n-p-n bipolar transistor is formed integrally with a lateral MOSFET. A **gate electrode** (36) is formed on an insulating layer (34) over a part of the **channel** region (32) which is in the base region.

ADVANTAGE - 'On' resistance of device, compared with previous combined bipolar-field effect transistor, is between one tenth and one third of previous value. In addition device is faster and provides enhanced lateral isolation.

1/5

Abstract (Equivalent): EP 146181 B

A p-type **semiconductor** substrate (11) has a lightly-doped (3.10.14) epitaxial buried layer (16) on its major surface, which is about thrity microns thick and is p-conductivity type. An n-type epitaxial surface layer (18), of doping concentration and thickness chosen according to the **reduced surface field** technique, is disposed in the buried layer (16). A surface adjoining p-conductivity base region (20) has a base electrode (22) and forms

05may04 15:32:12 User267149 Session D1374.1

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File 144:Pascal 1973-2004/Apr W4
(c) 2004 INIST/CNRS
File 305:Analytical Abstracts 1980-2004/Apr W4
(c) 2004 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.
File 315:ChemEng & Biotec Abs 1970-2004/Apr
(c) 2004 DECHEMA
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200427
(c) 2004 Thomson Derwent
*File 350: For more current information, include File 331 in your search. Enter HELP NEWS 331 for details.
File 347:JAPIO Nov 1976-2003/Dec(Updated 040402)
(c) 2004 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.
File 344:Chinese Patents Abs Aug 1985-2004/Mar
(c) 2004 European Patent Office
File 371:French Patents 1961-2002/BOPI 200209
(c) 2002 INPI. All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.

Set	Items	Description
S1	196	AU=(KINZER, D? OR KINZER D?)
S2	38	AU=(SRIDEVAN, S? OR SRIDEVAN S?)
S3	6	S1 AND S2
S4	6	RD (unique items)
S5	5	S4 AND SEMICONDUCT?
S6	228	S1:S2
S7	222	S6 NOT S4
S8	108	S7 AND SEMICONDUCT?
S9	33	S8 AND (MOSGATE???? OR MOS()GATE???)
S10	14	S9 AND (TRENCH? OR HOLE? OR GROOVE? OR CHANNEL OR EDGE? OR FLUSH OR RIDGE?)
S11	11	RD (unique items)

5/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015724515
WPI Acc No: 2003-786715/200374
XRPX Acc No: N03-630455
Sleeper junction type **semiconductor** device has substrate with well consisting of alternate arrangement of N, P strips which are depleted, when blocking voltage is applied across substrate
Patent Assignee: KINZER D M (KINZ-I); SRIDEVAN S (SRID-I); INT RECTIFIER CORP (INRC)
Inventor: **KINZER D M; SRIDEVAN S**
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020149051	A1	20021017	US 2001834115	A	20010412	200374	B
US 6512267	B2	20030128	US 2001834115	A	20010412	200374	

Priority Applications (No Type Date): US 2001834115 A 20010412
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020149051	A1		11	H01L-029/76	
US 6512267	B2			H01L-029/78	

Abstract (Basic): US 20020149051 A1
Abstract (Basic):
NOVELTY - The device has a substrate (21) with well (23) consisting of alternate arrangement of N and P type stripes (40,41) having concentration higher than the substrate. When blocking voltage is applied across the substrate and length of wells, the depletion of N and P stripes occurs.
USE - Superfunction type **semiconductor** device.
ADVANTAGE - **Semiconductor** device with simple guard ring termination structure and high blocking voltage, is reduced.
DESCRIPTION OF DRAWING(S) - The figure shows the top view of the cells in the wafer.
wafer (20)
substrate (21)
cell (23)
N type stripes (40)
P type stripes (41)
pp; 11 DwgNo 6/10

5/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015160132
WPI Acc No: 2003-220660/200321
XRPX Acc No: N03-176074
Lateral superjunction **semiconductor** device for use as high side switch, has trenches with mesas and N diffusion lines with reduced surface field concentration of prescribed width and concentration
Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: **KINZER D M; SRIDEVAN S**
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020195627	A1	20021226	US 2001891727	A	20010626	200321	B

DE 10229146 A1 20030109 DE 1029146 A 20020628 200321
JP 2003115588 A 20030418 JP 2002186923 A 20020626 200335

Priority Applications (No Type Date): US 2001891727 A 20010626
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 20020195627 A1 10 H01L-031/62
DE 10229146 A1 H01L-029/78
JP 2003115588 A 22 H01L-029/78

Abstract (Basic): US 20020195627 A1
Abstract (Basic):
NOVELTY - Trenches (20-23) extending through P-region (13) into top of N region (12), has mesas of prescribed width and concentration. N diffusion lines (30) having reduced surface field (RESURF) concentration, is diffused into the walls and along the bottom of trenches. A gate electrode, source and base regions of a MOS gate structure is connected at one end of the trenches and drain of the MOS gate structure is connected to other end.
USE - Lateral superjunction **semiconductor** device e.g. MOSFET for use as high side switch.
ADVANTAGE - Since the trenches with mesas and N diffusion lines with RESURF concentration have prescribed thickness and concentration, during the application of voltage to drain, the mesas and N diffusion fully deplete under blocking voltage conditions, and thus allows an almost uniform electric field distribution along the trench length. By the use of resurf concentration, the voltage applied between the drain and source on the device withstands.
DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view of the lateral conductive superjunction **semiconductor** device.
n region (12)
p region (13)
Trenches (20-23)
N-diffusion lines (30)
pp; 10 DwgNo 3/12

5/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014687893
WPI Acc No: 2002-508597/200254
XRAM Acc No: C02-144637
XRPX Acc No: N02-402491
High voltage vertical conduction super-junction **semiconductor** device comprises body having spaced vertical trenches, and diffusion formed in interior surface of trenches
Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: **KINZER D M; SRIDEVAN S**
Number of Countries: 098 Number of Patents: 006
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
WO 200247171 A1 20020613 WO 2001US47275 A 20011203 200254 B
US 20020070418 A1 20020613 US 2000732401 A 20001207 200254
JP 2002217415 A 20020802 JP 2001374875 A 20011207 200255
AU 200228895 A 20020618 AU 200228895 A 20011203 200262
US 6608350 B2 20030819 US 2000732401 A 20001207 200356
DE 10196990 T 20031023 DE 1096990 A 20011203 200373
WO 2001US47275 A 20011203

Priority Applications (No Type Date): US 2000732401 A 20001207
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200247171	A1	E	15	H01L-029/78	
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW				
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW					
US 20020070418	A1			H01L-023/58	
JP 2002217415	A		6	H01L-029/78	
AU 200228895	A			H01L-029/78	Based on patent WO 200247171
US 6608350	B2			H01L-029/78	
DE 10196990	T			H01L-029/78	Based on patent WO 200247171

Abstract (Basic): WO 200247171 A1
Abstract (Basic):
NOVELTY - A high voltage vertical conduction super-junction **semiconductor** device comprises body (2) of one conductivity type, spaced vertical trenches (3) formed in body upper surface, diffusion (4) formed in trenches' interior surface, and metal-oxide-**semiconductor**(MOS) gated structure connected to top of body and each diffusion. The diffusion is of another conductivity type.
USE - As high voltage vertical conduction super-junction **semiconductor** device.
ADVANTAGE - The inventive device includes diffusion having thickness and concentration and body having width and concentration that are matched to insure full depletion of the diffusion and body when blocking voltage is applied to the body. It is capable of blocking very high voltages while having an ultra low on-resistance in the conduction mode.
DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of small portion of the inventive super-junction chip.
Body (2)
Trenches (3)
Diffusion (4)
pp; 15 DwgNo 2/3

5/3,AB/4 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07621737
LATERAL SUPERJUNCTION **SEMICONDUCTOR** DEVICE

PUB. NO.: 2003-115588 [JP 2003115588 A]
PUBLISHED: April 18, 2003 (20030418)
INVENTOR(s): **KINZER DANIEL M**
SRIDEVAN SRIKANT
APPLICANT(s): INTERNATL RECTIFIER CORP
APPL. NO.: 2002-186923 [JP 2002186923]
FILED: June 26, 2002 (20020626)
PRIORITY: 01 891727 [US 2001891727], US (United States of America), June 26, 2001 (20010626)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a new lateral conductive type superjunction MOSFET device.

SOLUTION: Laterally extending trenches 20 to 23 are arranged at intervals in a P- region. An N- diffusion region is arranged along walls of trenches 20 to 23 so that the concentration and thickness of the N- diffusion region and a P- mesa are depleted fully during reverse blocking operation. The MOS gate structure is joined to one edge of the trenches 20 to 23 and the drain is connected to the other end of thereof. The other N- layer or the insulting oxide layer can be arranged between the P-- substrate 11 and the P- region 13.

5/3,AB/5 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

07348924
HIGH-VOLTAGE PERPENDICULAR CONDUCTIVE SUPERJUNCTION **SEMICONDUCTOR** DEVICE

PUB. NO.: 2002-217415 [JP 2002217415 A]
PUBLISHED: August 02, 2002 (20020802)
INVENTOR(s): **KINZER DANIEL M**
SRIDEVAN SRIKANT
APPLICANT(s): INTERNATL RECTIFIER CORP
APPL. NO.: 2001-374875 [JP 2001374875]
FILED: December 07, 2001 (20011207)
PRIORITY: 00 732401 [US 2000732401], US (United States of America), December 07, 2000 (20001207)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a high-voltage perpendicular conductive superjunction **semiconductor** device which can block very high voltage and has very low on-resistance in conduction mode.

SOLUTION: This high-voltage perpendicular conductive superjunction **semiconductor** device is provided with a plurality of deep trenches 3 in one conductivity- type lightly doped body. The other conductive type diffusion region is formed at a depth and à concentration aligned with those of the body, on the wall of the trench 3, and both areas are fully depleted under reverse-direction blocking. A thin and long trench 12 is filled with a dielectric substance as the compound of a nitride layer and an oxide layer for example, that has a dimensional change in the horizontal direction aligned with changed dimension of silicon. The filler may be a high-resistance SIPOS that can ensure leakage current from a source to a drain to keep a uniform distribution of electric field along the total length of the trench during blocking.

11/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5188334 INSPEC Abstract Number: B9603-2560J-035
Title: The ES-MGBT: a new fast switching **MOS-gated** power bipolar transistor with conductivity-modulation by a positive feedback mechanism
Author(s): Ajit, J.S.; **Kinzer, D.M.**
Author Affiliation: Adv. Product Dev., Int. Rectifier Corp., El Segundo, CA, USA
Conference Title: Proceedings of the 7th International Symposium on Power Semiconductor Devices and ICs, ISPSD `95 (IEEE Cat. No.95CH35785) p. 159-63
Publisher: Inst. Electr. Eng. Japan, Tokyo, Japan
Publication Date: 1995 Country of Publication: Japan xvii+502 pp.
ISBN: 0 7803 2618 0 Material Identity Number: XX95-00956
Conference Title: Proceedings of International Symposium on Power Semiconductor Devices and IC`s: ISPSD `95
Conference Sponsor: Tech. Committee on Electron Devices Inst. Electr. Eng. Japan; IEEE Electron Devices Soc.; Tech. Group on Silicon Devices & Mater. Inst. Electron. Inf. & Commun. Eng. Japan
Conference Date: 23-25 May 1995 Conference Location: Yokohama, Japan
Language: English
Abstract: A new **MOS-gated** device structure called the ES-MGBT is described which consists of P/sup +/ and N/sup +/ emitters, both of which are in emitter-switched configuration. In the ES-MGBT, a P/sup +/ injector coupled to the drain potential by a vertical driver DMOSFET is used to inject **holes** . A novel cell design is used to divert the injected **holes** to conductivity modulate the driver DMOSFET resulting in a low on-state voltage drop by a positive feedback mechanism. In addition, the bipolar transistor components of the device are placed in an emitter-switched configuration by the cell design which results in fast switching, high avalanche capability, and fully gate controlled characteristics. 750 V ES-MGBT devices fabricated along with DMOSFET devices on the same wafer showed 25% improvement in current density at room temperature and 36% improvement at 75 degrees C at a forward drop of 3.5 V. The turn-off time of the ES-MGBT was 80 ns - equal to that of the DMOSFET.
Subfile: B

11/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

4837030 INSPEC Abstract Number: B9501-2560J-016
Title: The MGBT: a new **MOS-gated** power bipolar transistor
Author(s): Ajit, J.S.; **Kinzer, D.M.**
Author Affiliation: Int. Rectifier Corp., El Segundo, CA, USA
Journal: IEEE Electron Device Letters vol.15, no.11 p.469-71
Publication Date: Nov. 1994 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
U.S. Copyright Clearance Center Code: 0741-3106/94/$04.00
Language: English
Abstract: A new device called the MGBT is described in which the upper regions of the device structure are conductivity-modulated by a positive feedback mechanism to give a lower on-state voltage drop compared to a power DMOSFET while having fast switching and fully gate-controlled

characteristics. In the MGBT, a P/sup +/ injector coupled to the drain potential by a vertical driver DMOSFET in an emitter-switched configuration is used to inject **holes** which is then diverted to the entire surface region of the device by a novel cell design. 750 V MGBT devices fabricated along with DMOSFET devices on the same wafer showed 33% improvement in current density at room temperature and 46% improvement at 75 degrees C at a forward drop of 3.5 V. The turn-off time of the MGBT was 80 ns equal to that of the DMOSFET.
Subfile: B

11/3,AB/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04269028
E.I. No: EIP95102893282
Title: New **MOS-gate** controlled thyristor (MGCT)
Author: Ajit, J.S.; **Kinzer, D.M.**
Corporate Source: Advanced Product Development, El Segundo, CA, USA
Conference Title: Proceedings of the 1995 IEEE International Symposium on Power Semicomductor Devices and ICs
Conference Location: Yokohama, Jpn Conference Date: 19950523-19950525
E.I. Conference No.: 43789
Source: IEEE International Symposium on Power Semiconductor Devices & ICs (ISPSD) 1995.,95CH35785. p 123-128
Publication Year: 1995
CODEN: PISDEK ISBN: 0-7803-2619-9
Language: English
Abstract: A new three-terminal power device structure called **MOS-Gate** Controlled Thyristor (MGCT) is described. The device consists of a thyristor structure with the thyristor current constrained to flow via the **channel** region of an enhancement-mode MOSFET. This allows limiting of the thyristor current by the MOSFET. The new structure does not have any parasitic thyristor structure. Multi-cell MGCT devices were fabricated along with IGBT devices on the same wafer showed about 20% improvement in on-state voltage drop over IGBT for 750 V devices. (Author abstract) 13 Refs.

11/3,AB/4 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014860521
WPI Acc No: 2002-681227/200273
XRAM Acc No: C02-192196
XRPX Acc No: N02-537693
Integrated metal oxide **semiconductor** gated device and Schottky diode structure has monocrystalline silicon die, **channel** diffusion layer, source layer, spaced **trenches**, source and drain electrodes, and planar Schottky metal layer
Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: **KINZER D M**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6433396	B1	20020813	US 99157740	A	19991005	200273	B
			US 2000679007	A	20001004		

Priority Applications (No Type Date): US 99157740 P 19991005; US 2000679007 A 20001004
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6433396	B1		6	H01L-029/94	Provisional application US 99157740

Abstract (Basic): US 6433396 B1
Abstract (Basic):

NOVELTY - An integrated metal oxide **semiconductor** gated device and Schottky diode structure comprises a monocrystalline silicon die, a **channel** diffusion layer, a source layer, spaced **trenches**, a conductive gate material filled in the **trenches**, a source electrode, a drain electrode, and a planar Schottky metal layer on top of and in contact with the body of the silicon die.

DETAILED DESCRIPTION - An integrated metal oxide **semiconductor** (**MOS**) **gated** device and Schottky diode structure comprises a die (30) of monocrystalline silicon of a first conductivity type. A **channel** diffusion layer (33) of a second conductivity type is formed into a first area of the top surface of the die. A source layer (61) of the first conductivity type is formed over the **channel** diffusion layer and extends to the top surface. Spaced **trenches** are provided which extend through the source layer and the **channel** diffusion layer. The interior walls of the spaced **trenches** are lined with a gate oxide (40). A conductive gate material (41) fills the interior of each of the **trenches**. A conductive source electrode is located on the top surface of the die and in contact with the source layer regions and **channel** diffusion regions of each of the **trenches**. A conductive drain electrode is coupled to the body of the die. A planar Schottky metal layer is locate on the top of and in contact with the body of the silicon die and extends over a second area of the top surface of the die. The first conductive source electrode extends across and in contact with the Schottky metal layer and serves as the anode contact for the Schottky barrier formed by the Schottky metal. The conductive drain electrode serves as the cathode contact of a Schottky diode formed by the Schottky metal layer. A gate electrode is connected to the conductive gate material.

USE - As an integrated **MOS gated** device (e.g., MOS field effect transistor) and Schottky diode structure.

ADVANTAGE - The structure has **MOS-gated** device and Schottky diode that are inherently connected in parallel and that share a common drain/cathode and a common source/anode, and thus can be manufactured easily and inexpensively.

DESCRIPTION OF DRAWING(S) - The figure illustrates a portion of the integrated **MOS gated** device and Schottky diode structure.

Die (30)
Channel diffusion layer (33)
Gate oxide (40)
Conductive gate material (41)
Source layer (61)
pp; 6 DwgNo 6/9

11/3,AB/5 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013179981
WPI Acc No: 2000-351854/200031
XRPX Acc No: N00-263594

Semiconductor component with **MOS gate** control used for battery powered, portable electronic components, e.g. laptop computers

Patent Assignee: INT RECTIFIER CORP (INRC)

Inventor: **KINZER D M**

Number of Countries: 004 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 19949364	A1	20000427	DE 1049364	A	19991013	200031 B
JP 2000156503	A	20000606	JP 99293015	A	19991014	200035
TW 437066	A	20010528	TW 99117761	A	19991014	200172
US 6476443	B1	20021105	US 98104148	P	19981014	200276
			US 99416796	A	19991013	
JP 3365984	B2	20030114	JP 99293015	A	19991014	200308
US 20030008445	A1	20030109	US 98104148	P	19981014	200311
			US 99416796	A	19991013	
			US 2002242015	A	20020911	
US 6610574	B2	20030826	US 98104148	P	19981014	200357
			US 99416796	A	19991013	
			US 2002242015	A	20020911	

Priority Applications (No Type Date): US 98104148 P 19981014; US 99416796 A 19991013; US 2002242015 A 20020911

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19949364	A1		18	H01L-029/78	
JP 2000156503	A		47	H01L-029/78	
TW 437066	A			H01L-027/105	
US 6476443	B1			H01L-029/76	Provisional application US 98104148
JP 3365984	B2		11	H01L-029/78	Previous Publ. patent JP 2000156503
US 20030008445	A1			H01L-021/336	Provisional application US 98104148
					Div ex application US 99416796
					Div ex patent US 6476443
US 6610574	B2			H01L-021/336	Provisional application US 98104148
					Div ex application US 99416796
					Div ex patent US 6476443

Abstract (Basic): DE 19949364 A1

Abstract (Basic):

NOVELTY - The component comprises a first conductivity substrate with top, flat surface. A **channel** diffusion region of a second conductivity extends in the substrate surface down to a first depth. A source diffusion region of second conductivity extends in the substrate surface down to a second smaller depth. Numerous, spaced **grooves** are formed in the substrate to a third depth, greater than first one, under the surface.

DETAILED DESCRIPTION - The **groove** sides are lined with an insulating film, while a conductive gate material fills the **grooves**. A source contact is coupled to source diffusion region on the surface and is laterally spaced from the **grooves**. A gate electrode is coupled to gate material, and a drain contact is coupled to the substrate. INDEPENDENT CLAIMS are included for the manufacture of the **semiconductor** component.

USE - For components, e.g. MOSFETs used in battery powered portable electronic apparatus, such as laptop computers etc.

DESCRIPTION OF DRAWING(S) - The figure shows cross-section of active region of **semiconductor** chip with buried structure and polysilicon gate.

pp; 18 DwgNo 5/14

11/3,AB/6 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013110534
WPI Acc No: 2000-282405/200024
Related WPI Acc No: 2004-019610
XRPX Acc No: N00-212544

Semiconductor package in which source of a metal-oxide-**semiconductor** field effect transistor **semiconductor** die is disposed between upper and lower plate members and is electrically connected to a lead frame

Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: CHEAH C; **KINZER D**; MUNOZ J

Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6040626	A	20000321	US 98101810	P	19980925	200024 B
			US 99225153	A	19990104	
JP 2000114445	A	20000421	JP 99273424	A	19990927	200031
TW 425682	A	20010311	TW 99116356	A	19990923	200143
JP 3240292	B2	20011217	JP 99273424	A	19990927	200203

Priority Applications (No Type Date): US 98101810 P 19980925; US 99225153 A 19990104
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6040626	A		15	H01L-023/48	Provisional application US 98101810
JP 2000114445	A		10	H01L-023/48	
TW 425682	A			H01L-023/495	
JP 3240292	B2		9	H01L-023/48	Previous Publ. patent JP 2000114445

Abstract (Basic): US 6040626 A
Abstract (Basic):

NOVELTY - The beam portion (34) of a **semiconductor** package (110) is preferably integrally formed into one flowing member extending from the lateral **edge** of a plate portion (30) to terminals (12b). A metallized region (19) defines a gate of the metal-oxide-**semiconductor** field effect transistor (MOSFET) die (16) and is electrically coupled to one terminal via a wire bond (20). A mixed connection to the MOSFET die top surface is used, namely a low resistance plate part (20) for connection to the source and the wire bond for connecting to the gate (19).

USE - Electrically coupling **semiconductor** die to a lead frame via upper plate member.

ADVANTAGE - Reducing resistance of current paths through **MOS gated** device and reducing inductances of such current paths.

DESCRIPTION OF DRAWING(S) - The drawing is a top plan view of an alternative embodiment of the **semiconductor** package

Beam portion (34)
Semiconductor package (110)
Plate portion (30)
Gate region (19)
MOSFET die (16)
Terminals (12b)
Wire bond (20)
pp; 15 DwgNo 4/9

11/3,AB/7 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012422555
WPI Acc No: 1999-228663/199919
XRAM Acc No: C99-067276
XRPX Acc No: N99-169157

Integrated Schottky diode and **MOS gated** device, especially a synchronous rectifier

Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: **KINZER D M**

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5886383	A	19990323	US 97782568	A	19970110	199919	B

Priority Applications (No Type Date): US 97782568 A 19970110
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5886383	A		8	H01L-029/76	

Abstract (Basic): US 5886383 A
Abstract (Basic):

NOVELTY - Schottky contact is formed by an aluminum contact layer (22) formed over an insulated gate (20, 21), and contacting the underlying chip (9). The surface of the chip has an invertible **channel** region formed in it, with source (14, 15) and drain regions.

DETAILED DESCRIPTION - A power **MOS gated** device comprises annular diffusion regions including an invertible **channel** region. It is in the surface of a **semiconductor** chip, with source and drain regions connected to different sides of the invertible **channel** region. A second diffusion region is formed directly beneath and contacting the entire bottom surface of the source, and being more heavily doped than the annular diffusion region, although narrower and shallower. An insulated gate is formed on the invertible **channel** region, to invert it under certain conditions. An annular shaped notch is formed in the surface of the chip, and extends from the surface through the source and into the second diffusion region. A contact metal is formed on the source and in the notch, contacting the source at the top of the chip, and also to the surface of the chip within the notch, forming a Schottky contact in parallel with the **MOS gated** device.

USE - For forming a synchronous rectifier.

ADVANTAGE - High speed Schottky diode is in parallel with a MOSFET, reducing recovery losses, and speeding recovery in the device.

DESCRIPTION OF DRAWING(S) - The figures show a cross-section of the chip, and the circuit symbol for it.

chip (9)
N- epitaxial body (10)
annular N+ source (14,15)
polysilicon gate mesh (20)
oxide (21)
source contact (22)
drain contact (29)
low loss Schottky diode (31)
P bases (40,41,42)
central openings in P bases (44,45)
pp; 8 DwgNo 3,3a/12

11/3,AB/8 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011372426
WPI Acc No: 1997-350333/199732
XRPX Acc No: N97-290400

Power insulated gate bipolar transistor device - has very deep increased concentration region between spaced bases of transistor and lifetime killing radiation dose applied to wafer

Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: **KINZER D M**

Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5644148	A	19970701	US 92945106	A	19920915	199732	B
			US 94364514	A	19941227		
			US 95461509	A	19950605		
			US 96674982	A	19960703		
IT 1272567	B	19970623	IT 93MI1898	A	19930903	199811	

Priority Applications (No Type Date): US 92945106 A 19920915; US 94364514 A 19941227; US 95461509 A 19950605; US 96674982 A 19960703
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5644148	A		21	H01L-029/74	Cont of application US 92945106
					Cont of application US 94364514
					Cont of application US 95461509
IT 1272567	B			H01L-000/00	

Abstract (Basic): US 5644148 A

The power transistor device has bipolar device forward current carrying characteristics and **MOS gate** control characteristics. The device includes a substrate (300) and a layer of **semiconductor** material (301) positioned on the substrate. The **semiconductor** material is of a first conductivity type and is lightly doped and has an upper surface. At least two spaced base regions (310,311) of opposite conductivity type extend into the upper surface of the layer of **semiconductor** material of first conductivity type to a given depth. At least two source regions (312,313) of the first conductivity type are formed in respective spaced base regions and define at least one surface **channel** region between them. A gate insulation layer (315) is positioned over the **channel** region. A conductive gate layer (113) is positioned over the gate insulation layer. A first main electrode is connected to the source regions. A further region of conductivity type opposite the first conductivity type extends into the upper surface of the **semiconductor** material of first conductivity type and spaced lateral distance away from the spaced base regions.

A second main electrode is connected to the further region of opposite conductivity type. The region between the spaced base regions includes an increased conductivity region with an increased concentration of carriers of the first conductivity type which extends from the upper surface of the **semiconductor** material to a depth greater than the depth of the spaced base regions. The increased concentration is greater than that of the remaining portion of the layer of **semiconductor** material over the full depth of the increased concentration region and is greater than twice that of the

remaining portion of the layer of **semiconductor** material in a portion of the increased conductivity region that is adjacent of the upper surface.

ADVANTAGE - Increases speed at which transistor may be switched by increasing space between base regions forming junction pattern.

Dwg.22/22

11/3,AB/9 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010895758
WPI Acc No: 1996-392709/199639
XRPX Acc No: N96-330953
Insulated gate bipolar transistor - has P-type collector diffusion region formed in N- drift region being spaced from P- resurf diffusion region and having N+ collector region formed within it to define second invertible **channel**
Patent Assignee: INT RECTIFIER CORP (INRC)
Inventor: **KINZER D M**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5548133	A	19960820	US 94308556	A	19940919	199639	B

Priority Applications (No Type Date): US 94308556 A 19940919
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5548133	A		7	H01L-029/74	

Abstract (Basic): US 5548133 A

The IGBT includes a thin **semiconductor** wafer with a P+ substrate extending to one wafer surface with a P- body formed atop it and extending to another wafer surface. At least one P-type base region is diffused into the P- body and an N-type emitter diffusion region formed in this base region to define an invertible **channel** region. A **MOS-gate** structure is disposed atop this invertible **channel** region.

An N- drift region is diffused into the P- body surface and it extends from the base region into which a relatively thick P- resurf diffusion region is formed and contained. A P-type collector diffusion formed in the drift region at a location spaced from the resurf diffusion region has an N+ collector diffusion region is formed in it to define a second invertible **channel** region between the N+ collector diffusion and N- drift regions upon which a second **MOS-gate** is disposed. Emitter and collector contacts are connected to the base and the P-type and N+ collector diffusion regions. Avalanche breakdown occurs from the P-type collector diffusion region to prevent avalanche breakdown from the P-type base region.

ADVANTAGE - Has improved ruggedness. Short circuit protection and overtemperature protection circuits are also integrated into chip. P+/N region causes breakdown to occur beneath P+ region away from critical **MOS-gate** region.

Dwg.4/5

11/3,AB/10 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008830818
WPI Acc No: 1991-334834/199146
Related WPI Acc No: 1998-361716
XRPX Acc No: N91-256566
Power transistor device having deep increased concentration region - forms increased conduction region before body and source regions, between spaced base and deeper than base region
Patent Assignee: INT RECTIFIER CORP (INRC); MERRILL P (MERR-I); IBM CORP (IBMC)
Inventor: GOULD H J; MERRILL P; MERRIL P; **KINZER D M**
Number of Countries: 009 Number of Patents: 015
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2243952	A	19911113	GB 9110071	A	19910509	199146	B
DE 4114174	A	19911114	DE 4114174	A	19910430	199147	
FR 2662025	A	19911115				199205	
CA 2042069	A	19911110				199206	
JP 4229660	A	19920819	JP 91104491	A	19910509	199240	
FR 2695253	A1	19940304	FR 915460	A	19910503	199415	
			FR 9310793	A	19930910		
GB 2243952	B	19940817	GB 9110071	A	19910509	199430	
IT 1247293	B	19941212	IT 91MI1121	A	19910423	199520	
US 5661314	A	19970826	US 90521177	A	19900509	199740	
			US 9341136	A	19930330		
			US 94316112	A	19940930		
AT 9100956	A	19980415	AT 91956	A	19910508	199820	
AT 404525	B	19981015	AT 91956	A	19910508	199846	
KR 9511019	B1	19950927	KR 917564	A	19910509	199848	
US 5904510	A	19990518	US 90521177	A	19900509	199927	
			US 9341136	A	19930330		
			US 94316112	A	19940930		
			US 97807387	A	19970227		
JP 3004077	B2	20000131	JP 91104491	A	19910509	200010	
DE 4143660	A1	20010104	DE 4114174	A	19910430	200103	
			DE 4143660	A	19910430		

Priority Applications (No Type Date): US 90521177 A 19900509; US 9341136 A 19930330; US 94316112 A 19940930; US 97807387 A 19970227
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2243952	A		57		
JP 4229660	A		18	H01L-029/784	
FR 2695253	A1			H01L-021/74	Div ex application FR 915460
GB 2243952	B		2	H01L-029/06	
IT 1247293	B			H01L-000/00	
US 5661314	A		20	H01L-029/10	Cont of application US 90521177 Cont of application US 9341136
AT 9100956	A			H01L-029/78	
AT 404525	B			H01L-029/78	Previous Publ. patent AT 9100956
KR 9511019	B1			H01L-029/78	
US 5904510	A			H01L-021/00	Cont of application US 90521177 Cont of application US 9341136 Div ex application US 94316112 Div ex patent US 5766966
JP 3004077	B2		17	H01L-029/78	Previous Publ. patent JP 4229660
DE 4143660	A1			H01L-029/739	Div ex application DE 4114174 Div ex patent DE 4114174

Abstract (Basic): GB 2243952 A

The cellular insulated gate bipolar transistor (''IGBT'') device employs increased concentration in the active region (60,61,62) between spaced base (80,81,82) to a depth greater than the depth of the base regions. The ion implant dose which is the source of the increased concentration is about 3.5 x 10 (power 12) atoms per centimeter squared and is diffused for about 10 hours at 1175 deg.C. Carrier lifetime is reduced by an increased radiation dose.

The increased concentration region (60,61,62) permits a reduction in the spacing between bases (80,81,82) and provides a region of low localised bipolar gain, increasing the device latch current. The very deep increased conduction region is formed before the body and source regions in a process for making the new junction pattern.

ADVANTAGE - Reduced switching loss, avalanche energy successfully absorbed while turning off inductive load is increased.

Dwg.19/22

Abstract (Equivalent): GB 2243952 B

A power transistor device having bipolar device forward current carrying characteristics and **MOS gate** control characteristics; said device comprising a chip of **semiconductor** material having a substrate of one conductivity type, a lightly doped layer of **semiconductor** material of the opposite conductivity type disposed atop one surface of said substrate, a plurality of spaced base regions of said one conductivity type extending into the opposite surface of said layer of **semiconductor** material to a given depth, a plurality of source regions of said -opposite conductivity type formed in respective ones of said plurality of spaced base regions and defining respective surface **channel** regions, a gate insulation layer disposed over said **channel** regions, a conductive gate layer disposed over said gate insulation layer, a first main electrode connected to said plurality of source regions and a second main electrode connected to said substrate, the regions between said spaced base regions having an increased concentration of carriers of said opposite conductivity type which extends from said opposite surface to a depth greater than the depth of said base regions; said increased concentration being greater than that of the remaining portion of said layer of **semiconductor** material over its full depth.

Dwg.1

Abstract (Equivalent): US 5661314 A

A power transistor device having bipolar device forward current carrying characteristics and **MOS gate** control characteristics; said device comprising a thin chip of **semiconductor** material having a substrate of one conductivity type, a lightly doped layer of **semiconductor** material of the opposite conductivity type disposed atop one surface of said substrate, a plurality of spaced base regions of said one conductivity type extending into the opposite surface of said layer of **semiconductor** material to a given depth, a plurality of source regions of said opposite conductivity type formed in respective ones of said plurality of spaced base regions and defining respective surface **channel** regions, a gate insulation layer disposed over said **channel** regions, a conductive gate layer disposed over said gate insulation layer, a first main electrode connected to said plurality of source regions and a second main electrode connected to said substrate, the regions between said spaced base regions having an increased concentration of carriers of said opposite conductivity type which extends from said opposite surface to a depth greater than the depth of said base regions; said increased concentration being greater than that of the remaining portion of said layer of **semiconductor** material over its full depth.

Dwg.19/22

11/3,AB/11 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05946093
MANUFACTURE OF P-**CHANNEL MOS GATE** CONTROL DEVICE WITH BASE INJECTED THROUGH CONTACT WINDOW AND **SEMICONDUCTOR** DEVICE

PUB. NO.: 10-229193 [JP 10229193 A]
PUBLISHED: August 25, 1998 (19980825)
INVENTOR(s): **KINZER DANIEL M**
APPLICANT(s): INTERNATL RECTIFIER CORP [178639] (A Non-Japanese Company or Corporation), US (United States of America)
APPL. NO.: 09-315466 [JP 97315466]
FILED: November 17, 1997 (19971117)
PRIORITY: 7-31,051 [US 31051-1996], US (United States of America), November 18, 1996 (19961118)